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(54) **Dynamic random access memory device, and a memory cell therefor**

(57) A dynamic RAM cell comprises a substrate (104) of one conductivity type in which is formed a first region (101) of a second and opposite conductivity type and a first pocket (102) of the second conductivity type having formed therein a second pocket (103) of the same conductivity type as the substrate but of a higher doping concentration than the substrate. By forming a channel (114) between the first region and the first pocket, the charge in the first pocket (102) can be controlled to represent a selected bit of information. The magnitude of charge stored in the first pocket (102) can then be determined by forming a channel across the first pocket to the second pocket from the substrate. The rate of change of the potential in the second pocket is representative of the stored charge of information in the first pocket due to the fact that the impedance of the channel formed across the first pocket is directly related to the amount of charge stored in the first pocket.

FIG. 1A

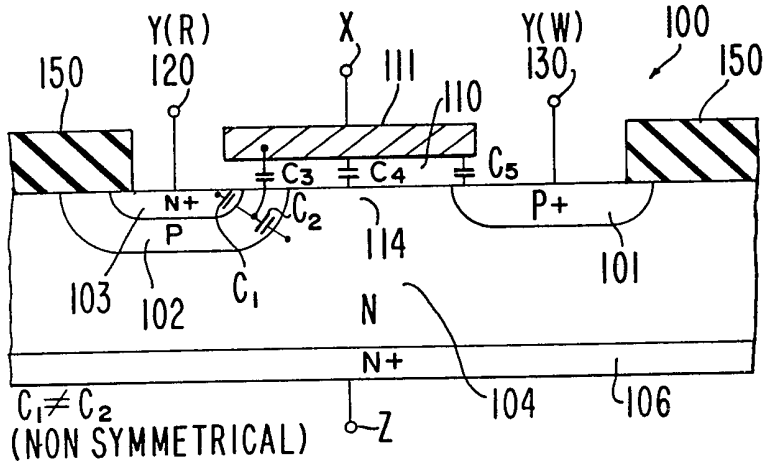

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FIG. 1A

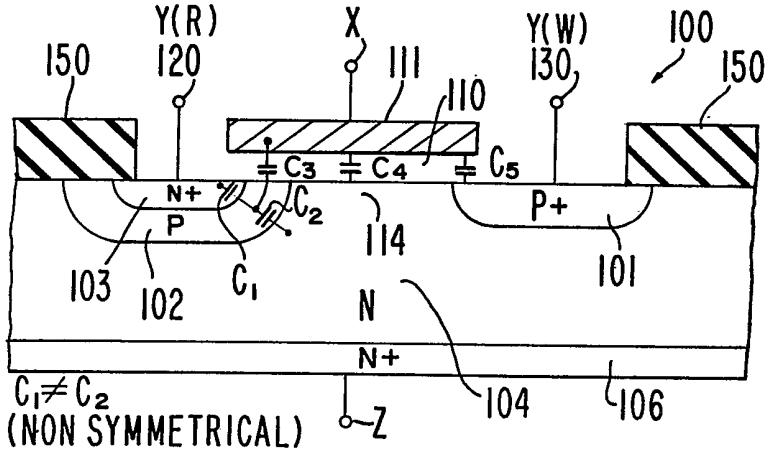

FIG. 2A

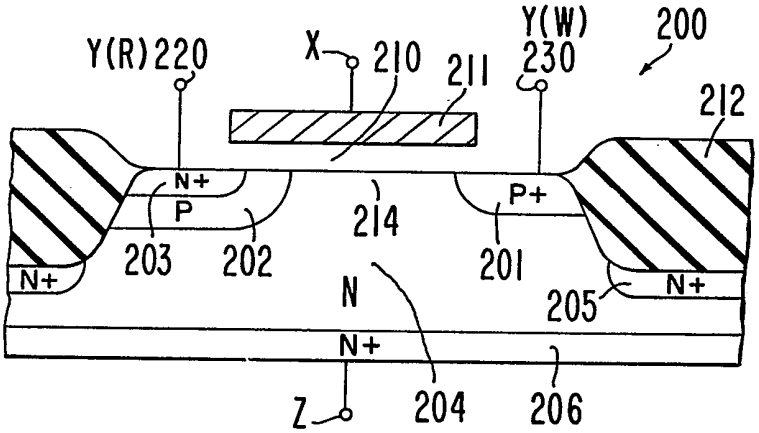

FIG. 3A

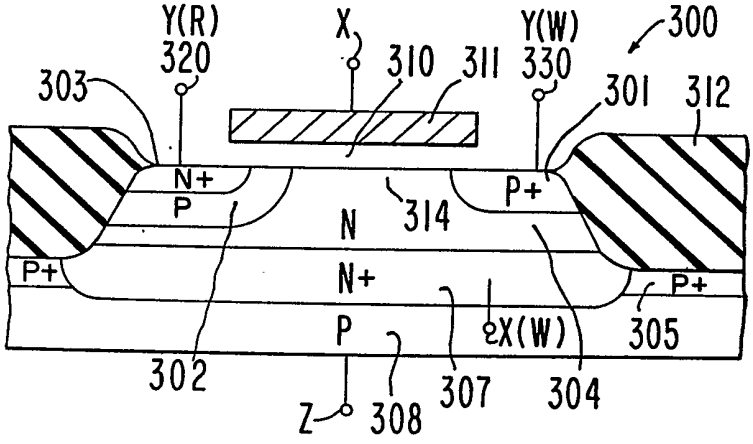

FIG. 4A

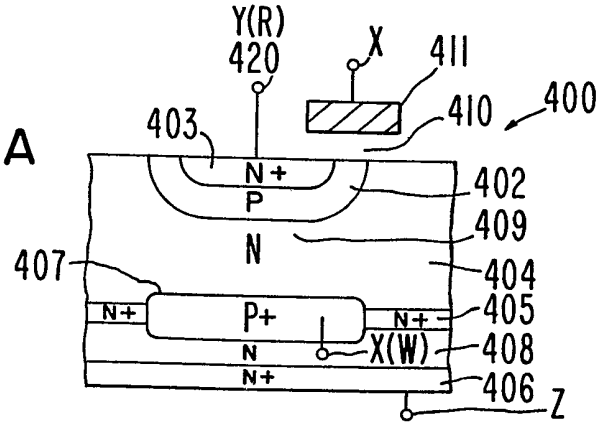

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FIG. 1B

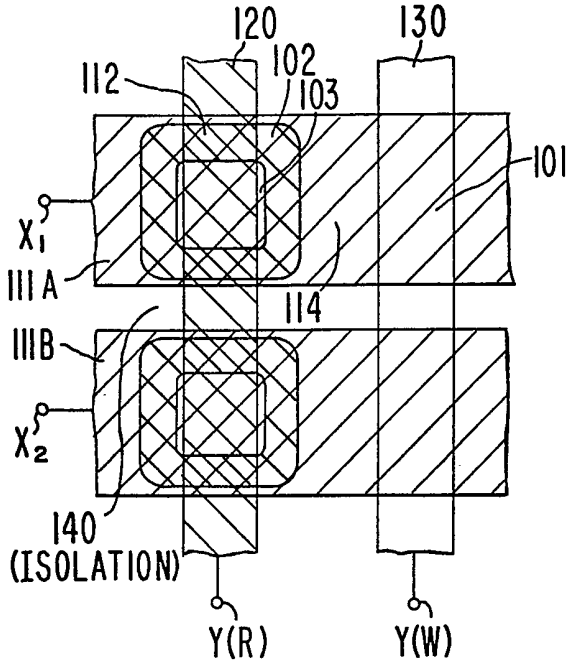

FIG. 2B

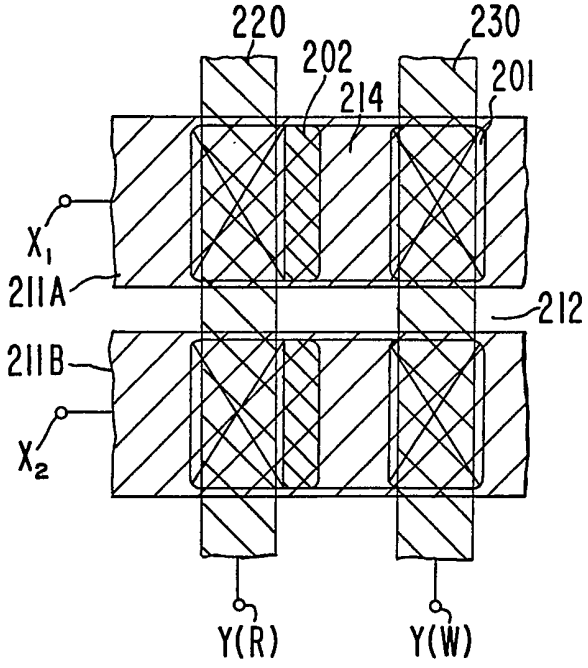

FIG. 4B

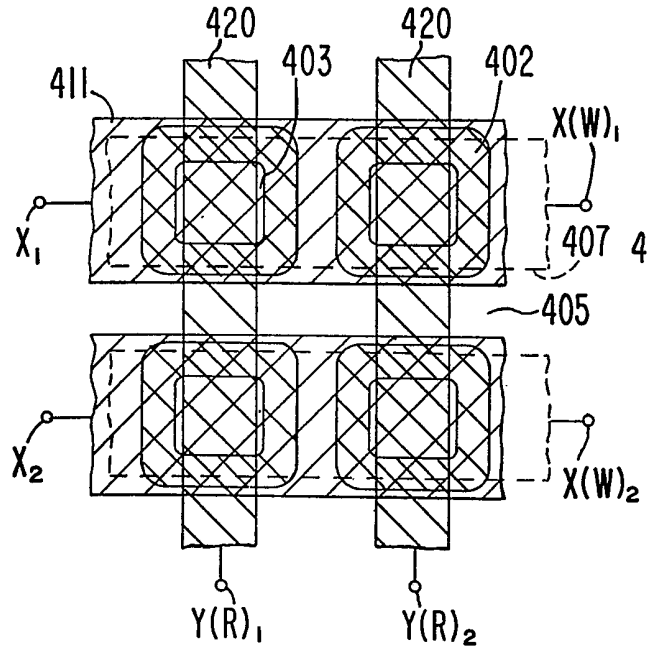

FIG. 4C

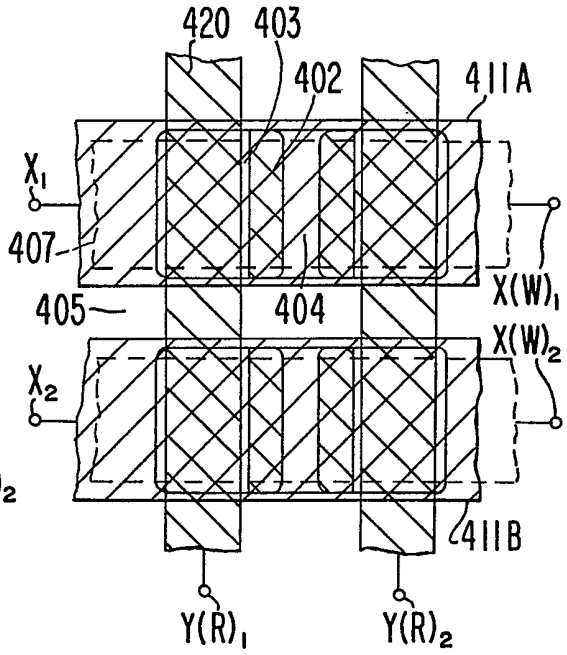

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FIG. 5

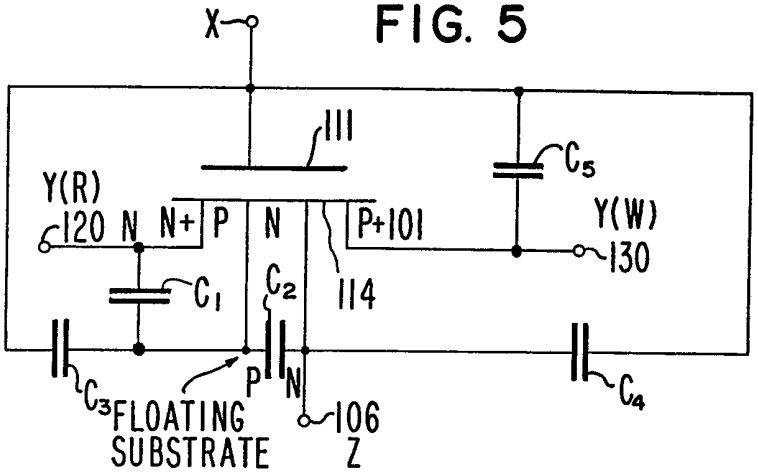


FIG. 6

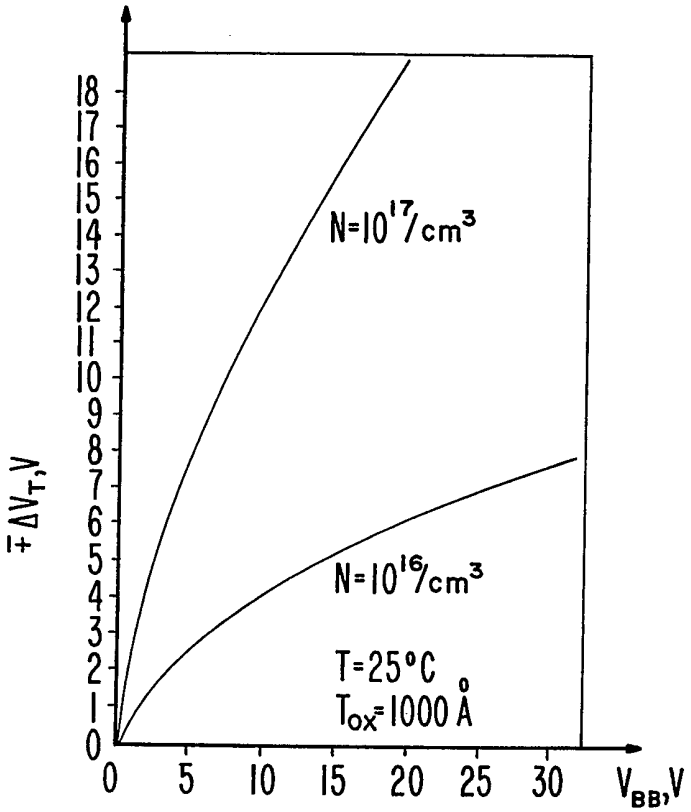
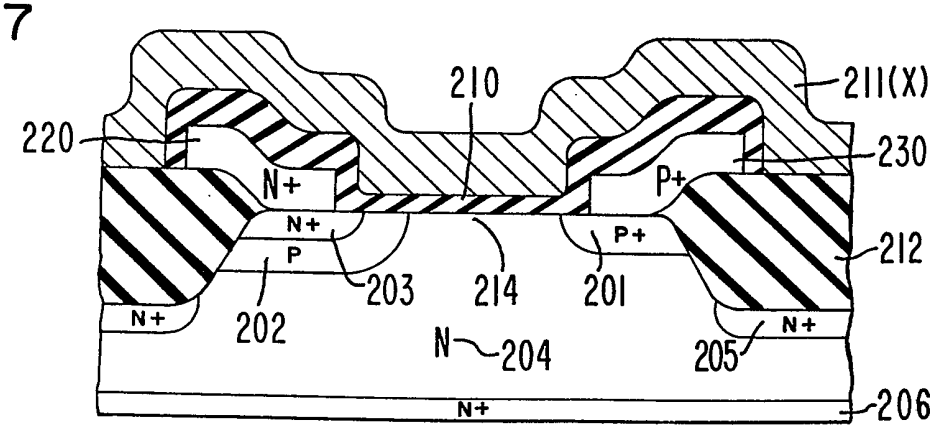


FIG. 7



SPECIFICATION

Dynamic random access memory device, and a memory cell therefor

This invention relates to a dynamic random access memory (DRAM) device and a memory cell therefor.

High density dynamic random access memories are well known in the art. An article entitled "A survey of High Density Dynamic Ram Cell Concepts" published by the IEEE Translations on Electron Devices, Volume ed.-26, No. 6, June, 1979, describes a variety of dynamic RAM cell concepts and compares these concepts to the industry's standard N Channel, MOS Dynamic RAM (DRAM) Cell. The prior art DRAMS store information in the form of the presence or absence of a charge packet stored on a single capacitor accessed by a single transistor. In very high density DRAM arrays, the geometrical area of the storage capacitor is very small, making detection of the presence or absence of the charge packet exceedingly difficult. For example, state of the art DRAM arrays utilize sense amplifiers which must be capable of sensing signals of less than 100 millivolts magnitude. This makes such arrays extremely susceptible to process variations as well as to spurious signals and external influences such as alpha particle radiation.

According to one aspect of the invention, there is provided a semiconductor memory cell comprising: a semiconductor substrate of a first conductivity type; a first region of a second conductivity type formed in said semiconductor substrate; a second region of said first conductivity type formed in said first region; a third region of said second conductivity type formed in said substrate spaced from said first region; means for applying selected potentials to said first, second and third regions and said substrate; and a conductive gate formed over, but insulated from, portions of said first region, and second region and said semiconductor substrate to enable a channel to be formed in said first region to connect said second region to said substrate.

According to a second aspect of the invention, there is provided a semiconductor memory cell comprising: a semiconductor substrate of a first conductivity type; a first region of a second conductivity type formed in said semiconductor substrate; a second region of said second conductivity type formed in said substrate spaced from said first region; first insulation formed over the region between said second region and said third region; a conductive gate formed on said first insulation over said space between said second region and said third region to form a first transistor from said first region, said third region and said substrate with a channel of said second conductivity type capable of being formed in said substrate and a second transistor from said second region, said substrate and said first region with a channel of said first conductivity type capable of being formed in said first region, said conductive gate comprising a common gate for both devices; and means applying selected potentials to said second and third regions, said conductive gate and said substrate to turn off one of said two transistors while turning on the other of said two transistors.

According to a third aspect of the invention there is provided a semiconductor memory device comprising a plurality of cells and selected peripheral circuitry including sense amplifiers, formed in a semiconductor substrate of a first conductivity type, each cell comprising: a first region of said first conductivity type formed in said semiconductor substrate for the storage of charge representative of information; a second region of said first conductivity type formed in said first region; a third region of said second conductivity type formed in said substrate spaced from said first region; and means for forming a conductive path between said first region and said third region, to control the charge stored in said first region in response to a first selected set of potentials applied to said substrate, said third region, said second region and said means for forming, and for forming a conductive channel from said second region to said substrate through said first region in response to a second selected set of potentials applied to said substrate, said third region, said second region and said means for forming, the rate of change of potential in said second region in response to said second set of potentials being indicative of the information stored in said first region.

Thus, the invention provides a DRAM cell which provides a transistor amplification of the stored charge packet, yet can be implemented in no lesser a packing density than prior art cells.

Further, the well-known variation of threshold voltage of a standard MOS transistor with substrate voltage V_{BB} is turned to advantage to produce a DRAM which has natural isolation and which lends itself to higher packing densities because it does not rely on the area of a capacitor for the storage of charge as do prior art DRAMs. Furthermore, a memory cell embodying the invention retains information for a longer time than do surface DRAMs and therefore exhibits less frequent need for refresh. Each transistor in a memory cell embodying this invention produces a larger signal than do prior art DRAM transistors and provides a non-destructive readout and a faster access to each transistor. Furthermore a semiconductor memory device embodying this invention provides almost complete immunity to alpha particle induced soft errors of the type which have plagued prior art dynamic RAMS.

In accordance with this invention, a DRAM cell comprises a substrate of one conductivity type in the top surface of which are formed a first region of a second and opposite conductivity type and a first pocket of this second conductivity type. The first pocket has formed therein a second pocket of the same conductivity type as the substrate, but of a higher doping concentration than the substrate. This second pocket comprises a bit line and the first pocket of opposite conductivity type in which the second pocket is formed comprises a storage region for charge. The first region of the same conductivity type as this storage region comprises a bit line for writing information into the storage cell. The substrate is selectively biased to provide the proper operating potential for the structure. Overlying the region between the first region and the first pocket (both

of opposite conductivity type) and a portion of the first pocket therefrom is a gate which comprises a word line.

In order that the invention may be readily understood, embodiments thereof will now be described, by way of example with reference to the accompanying drawings, in which:

Figure 1A is a sectional diagrammatic side view of a memory cell embodying the invention for use in forming a semiconductor memory array;

Figure 1B shows in plan view two of the memory cells of Figure 1 forming part of a semiconductor memory array;

Figure 2A is a sectional diagrammatic side view of a memory cell similar to that shown in Figure 1A but wherein recessed oxide isolation is provided between adjacent memory cells to increase the density of the array formed therefrom;

Figure 2B shows in plan view two of the memory cells of Figure 2A forming part of a semiconductor memory array;

Figure 3A is a sectional diagrammatic side view of a memory cell similar to that shown in Figure 2A having an additional buried isolation and interconnection layer and an epitaxial layer formed on top thereof in a manner analogous to the fabrication of a standard bipolar transistor;

Figure 4A is a sectional diagrammatic side view of a memory cell embodying the invention having a floating substrate programmed by punch-through from a buried diffusion which likewise uses in its fabrication an epitaxial layer and which can be fabricated using either junction isolation or recessed oxide isolation to enhance the packing density of the device;

Figure 4B is a plan view of four of the memory cells of Figure 4A forming array part of a semiconductor memory array;

Figure 4C is a plan view of part of a memory array formed using the memory cells of Figure 4A which memory cells have recessed oxide isolation;

Figure 5 illustrates schematically the relevant capacitances between the various elements of the memory cell shown in cross-section in Figure 1A;

Figure 6 illustrates graphically the dependence of the threshold voltage V_T of a MOS device on the source-to-substrate voltage V_{BB} of the device for various substrate doping concentrations; and

Figure 7 is a more detailed sectional side view of the memory cell of Figure 2A.

Standard N channel MOS devices have a common P type substrate. It is well-known that the substrate voltage V_{BB} influences the NMOS transistor threshold voltage. As shown in the book entitled "MOS Field-Effect Transistors and Integrated Circuits" by Paul Richman, published in 1973 by John Wiley & Sons, Inc., Section 2.3, page 32, the threshold voltage of MOS transistors varies with the applied substrate-to-source bias. As disclosed therein, the required threshold voltage changes both with dopant concentration and with the substrate-to-source voltage. This strong relationship is illustrated in Figure 6. Thus, with an N Channel MOS structure formed in a P type substrate, the more negative the substrate voltage V_{BB}, the higher the threshold voltage. This concept is used in the present invention for the storage of data in a dynamic RAM.

Embodiments of a memory cell in accordance with the invention are shown in Figures 1A, 2A, 3A, 4A and 7. It should be understood that other memory cells identical to the memory cell of 100 for example are formed in the same monolithic chip of silicon material to comprise together with peripheral circuitry a semiconductor memory device and that these other memory cells are identical in cross-section to the memory cell shown. In the memory cell 100 of Figure 1A, an N type semiconductor substrate 104 has formed on the bottom surface thereof an N+ type region of semiconductor material 106 for use in making ohmic contact to the substrate 104. Formed in the top surface of substrate 104 are P type region 102 and P+ type region 101. P type region 102 is a localized pocket, usually but not necessarily formed by diffusion, which typically has an impurity concentration ranging from 1×10^{15} atoms cm^{-3} to 1×10^{17} atoms cm^{-3} while P+ type region 101, typically formed in a separate operation such as a diffusion, is of higher conductivity having an impurity concentration in the range of about 1×10^{18} atoms cm^{-3} to 5×10^{19} atoms cm^{-3}. The impurity is preferably boron. Of course, other impurities and impurity concentrations for these two regions can be used as appropriate for the particular design goals of the memory cell. N+ type region 103 is formed in P type region 102 typically by diffusion, for example, using arsenic or phosphorous and has an impurity concentration in the range of from 1×10^{19} atoms cm^{-3} to 1×10^{20} atoms cm^{-3}. A field oxide layer 150 of a first selected thickness and a gate oxide layer 110 of a second, thinner selected thickness are formed over the top surface of the structure. Openings in the gate oxide 110 and the field oxide 150 allow the formation of electrical contacts 120 and 130 to N+ type region 130 and P+ type region 101, respectively. Electrical contacts 120 and 130 are electrically insulated from conductive gate 111 which is formed from any conductive material but preferably polysilicon or aluminium and which forms the gate of the memory cell and a word line in the semiconductor memory array.

Figure 1B is a plan view of two of the memory cells of Figure 1A forming part of a semiconductor array. As shown in Figure 1B, the P type well region 102 intersects the top surface of semiconductor substrate 104 to form a substantially rectangular band (tub) surrounding the N+ type region 103. Contact to the N+ type region 103 is made through a strip of conductive material forming the contact 120 which serves as the read line for the memory cells. Likewise, contact to the region 101 is made through a conductive strip which forms contact 130 and which serves as the write line for the memory cells. Naturally, contact strips 120 and 130 are insulated from those portions of the underlying semiconductor material to which electrical contact is not to

be made. The word lines 111A and 111B for two rows X_1 and X_2 respectively overlie but are insulated from both conductive strip 120 and conductive strip 130. Between each cell in rows X_1 and X_2, for example, is formed isolation 140 (Figure 1B) which is typically junction isolation, but, as will be seen shortly, can also be recessed oxide, otherwise known as an isoplanar-type isolation (see United States Patent 3,648,125 for a description of the isoplanar process and structure made thereby). Thus, as is apparent when Figures 1A and 1B are taken together, each memory cell has a single conductive strip word line X (111A or 111B in Figure 1B) which overlaps both P type region 102 and N+ region 103. The P type region 102 completely surrounds and isolates the N+ type region 103 which is accessed via a contact opening in its insulation to contact strip 120 (Y(R)), the column "read" line in Figure 1A. Preferably, contact strip 120 is an N+ type doped polycrystalline silicon line (Y(R)) which passes over thick field oxide in the regions between adjacent bits on the same Y column. No field isolation is required since the P type 102 is self-isolated. Typically, P type well 102 is formed as in the well-known depletion type MOS (DMOS) process by diffusion of boron through the same contact opening as is used to form N+ type region 103. Thus, the process is inherently simple in that a single opening serves as the diffusion mask for two diffusions. Such a process is shown, for example, in a paper entitled "A 4096 × 1 (1^3L)* BiPolar Dynamic RAM" by Wendell B. Sander and James M. Early published in the Transactions of the ISSCC, 76 on Friday, 20th February, 1976. This paper discloses the formation of a base region and an emitter region using a single diffusion in a bipolar process.

A region for contact by the second contact strip 130 (Y(W)), (the "write" column line) is formed by diffusing a P type impurity such as boron to provide a P+ type conductivity region 101. Of course, contact strip 130 can be a P+ type doped polycrystalline write line passing over thick field oxide in the regions between adjacent bits in the same Y column and contacting pockets comprising regions 101.

The substrate 104 as being N type conductivity, but may be formed from an N type epitaxial layer or an N+ type doped substrate.

In operation, the memory cell of Figures 1A and 1B is programmed by varying the potentials on word line 111 and the P+ type contact strip or write line 130. To write a "0", P type well 102 is placed at zero volts while to write a "1", P type well 102 is placed at a potential of about −3 volts. The P+NP transistor formed by regions 101, 104 and 102 is used to change the voltage of region 102 to either zero volts or −3 volts. To write a "0" into the transistor, for example, the voltage on conductive strip 120 (Y(R)) is held at zero volts, the gate voltage on X gate 111A is lowered to −5 volts to form a conductive P type channel connecting P type well 102 to P+ type well 102 and the potential on conductive strip 130 is held at zero volts thereby insuring that the potential of P type well 102 goes to zero volts. Accordingly, the channel inversion threshold of the N+PN MOS transistor formed from N+ type region 103, P type well 102 and N type substrate 104 becomes about 1.4 volts.

To write a "1" into the transistor, the above procedure is repeated except that the potential on conductive strip 130 is lowered to −3 volts. Accordingly, the potential in P type well 102 becomes −3 volts and the turn-on voltage threshold for the N+PN MOS transistor formed by regions 103, 102 and 104 becomes approximately +2.5 volts.

Once a bit of information (either a "0" or a "1") is stored in P type well 102, the regions 103, 102 and 104 are operated as an N type channel transistor with a P type well 102 serving as the P type substrate, N+ type region 103 and N type region 104 serving as the source and drain, respectively.

Once the gate voltage is removed from the gate 111 of the memory cell then the programing voltage is removed from conductive strip 130 and the P type well remains charged until the excess charge is lost either thermally or optically. This can take several milliseconds by which time a sense and refresh cycle is necessary as in other dynamic RAMS.

The reading out of the information stored in the cell is non-destructive and, unlike the read cycle is standard RAMs, is an active transistor read operation providing a much higher signal level than the capacitor charge dumping of standard RAMS. Reading occurs by charging conductive strip 120 (column "read line" Y(R)) which is electrically connected to one arm of a balanced sense amplifier (not shown) of a well-known design, to some positive voltage (such as +2.5 volts), raising the word line 111 (X) to about +5 volts and monitoring the rate of change of voltage of conductive strip 120 (Y(R)). If the N+PN MOS transistor formed by regions 103, 102 and 104 is in the high threshold state (that is, if its potential is at about −3 volts) the voltage change of conductive strip 120 (Y(R)) will be much slower than if the N+PN MOS transistor is in the low threshold state (*i.e.* with zero volts on P type well 102). The rate of change of voltage is compared with that of a reference cell attached to the other arm of the sense amplifier, which therefore causes it to flip and latch in a "0" or "1" state. The reading is non-destructive because the surface channel formed across the P type region 102 from N+ type region 103 to N type region 104 does not dischage the excess charge in P type well 102 since the PN junction between P type well 102 and this surface chanel is back biased. During this operation the substrate 104 is held at +5 volts by the application of the potential to N+ type semiconductor material contact region 106. The positive bias on the control gate 111A (X) shuts off the MOS transistor formed from P+type region 101, P type region 102 and N type substrate 104. Thus, the charge in P type well 102 is not allowed to discharge through a channel to P+ type well 101.

During the read and write operations, all unselected X word lines are at a voltage X = 0 volts. This potential keeps both the N channel and P channel MOS transistors formed by regions 103, 102 and 104, and by regions 102, 104 and 101, respectively, turned off.

One advantage of this structure is that the P type well 102 is naturally isolated since the substrate 104 is at

a higher voltage than the P type well, thereby back biasing the PN junction between these two regions. Thus the structure lends itself to shrinkage because it does not rely on the area of a capacitor for charge storage but rather merely on the charge stored in the volume of P type well 102. Furthermore, because generation-recombination of charge in surface states is substantially lower in a memory cell embodying the invention, the charge is held in P type well 102 for a longer period of time than with most surface dynamic RAMS, thereby decreasing refresh cycle frequency. The output signal from the memory cell embodying the invention is larger than the output signal from prior art DRAMs and the readout is non-destructive. Therefore a DRAM device embodying the invention provides a potentially faster access during the read operation than the prior art devices. Finally, because of the quantity of charge placed in P type well 102 and because of reverse-biased voltage conditions during storage, a DRAM device embodying the invention provides a potentially better immunity to soft errors due to radiation effects than prior art DRAM devices. Naturally, the above advantages are obtained partially as a result of disadvantages in other aread. Thus, the process used to make the device is potentially more complex because of the requirement for a P+ type diffusion to form P type region 101 and the P type well diffusion to form P type region 102. Moreover, to operate the device, negative as well as positive gate and diffusion voltages are required. However, these voltages can be provided in a relatively easy manner using the typical −5 volt supply and CMOS potential circuitry. The CMOS circuitry is particularly useful with this process because the process uses CMOS type processing steps in conjunction with the formation of P type well 102 and N+ type region 103 therein. Finally, although the read operation is non-destructive, a writing operation is destructive for the memory cell in unselected columns sharing the same row or X line such as line 111A as the selected memory cell. Therefore, a writing operation must be preceded by a read operation and latching of the stored data in all memory cells of the selected row so that the data can be written back into the cells during the subsequent write operation. This, however, is no different from what is now required in the operation of standard dynamic RAMS.

Figure 2A shows a memory cell identical to that shown in Figure 1A except that the isolation is formed by recessed oxide (just as in the isoplanar MOS process depicted in for example, U.S. Patent No. 3,913,211). The operation of this memory cell is precisely the same as the operation of the memory cell shown in Figure 1A. The main difference is that the isolation occurs partly as a result of the reverse biased PN junction between P type well 202 and N type substrate 204 and partly and a result of recessed oxide 212. Formed beneath recessed oxide 212 are N+ type channel stop regions 205 which serve, in a well-known manner, to prevent leakage paths from forming beneath the oxide. In addition, channel stop regions 205 also lower the substrate 204 resistance so that the read operation becomes more efficient.

Figure 2B shows in plan view two of the memory cells of Figure 2A forming part of a semiconductor memory array. A reduction in cell dimensions of the memory cell shown in Figure 2A relative to the memory cell of Figure 1A occurs as a result of the use of the isoplanar process for the formation of the memory cell. As shown in Figure 2B, oxide surrounds the P type well 202 on three sides, the fourth side comprising the channel region 214 between P type well 202 and P+ type well 201. Conductive strips 220 and 230 are shown in comparable locations to the corresponding conductive strips 120 and 130 in Figure 1B and conductive strips or word lines 211A and 211B are likewise shown in comparable locations to strips 111A and 111B in Figure 1B. Each of these elements serves the same function in the structure of Figure 2B corresponding element does in Figure 1B.

As is apparent from Figures 1A and 2A, corresponding elements in the two structures are denoted with corresponding numbers. Thus, P type well 102 in Figure 1A corresponds to P type well 202 in Figure 2A and N type substrate 104 in Figure 1A corresponds to N type substrate 204 in Figure 2A.

A further embodiment of a memory cell in accordance with the invention is shown in Figure 3A. The memory cell 300 is identical to the memory cell 200 shown in Figure 2A except that the cell is formed on a P type substrate 308 and employs an N+ type buried layer 307 which serves as the X(W) line and also serves, together with recessed oxide 312, to isolate each cell from adjacent cells. Thus, N+ type buried region 307 is formed in the top surface of P substrate 308 and an epitaxial layer 304 of N type conductivity is then formed on substrate 308. The recessed oxide regions 312 are then formed through the epitaxial layer and contact the N+ type buried layer 307 in a manner well known in the semiconductor arts and as ememplified in U.S. Patent No. 3,648,125, for example. P type well 302, P+ type region 301 and N+ type region 303 are then formed in the semi-conductor material 304 in a manner well known in the art. This remaining structure is fabricated in a manner similar to that disclosed in U.S. Patent No. 3,873,989 issued March 25, 1975 to Schinella et. al and entitled "Double Diffused Lateral Transistor Structure" but differs from this prior art memory cell by comprising an MOS structure rather than a bipolar structure and by employing gate 311.

Although the prior art has disclosed a memory cell having a "Bimos" structure a sectional diagrammatic side view of which is similar to that shown in Figure 1A, the prior art memory cell basically comprises a P channel MOS device made up of regions analogous to P type well 102, substrate 104 and P+ type region 101 (Figure 1A) and a bipolar NPN transistor made up of regions analogous to N+ type region 103, P type region 102 and N type substrate 104. This prior art memory cell uses a gate electrode corresponding in part to electrode 111 (but not extending over N+ type region 103) to control the base current to the NPN transistor. The P type channel formed between regions analogous to P type well 102 and P+ type region 101 provides a high impedance current path for controlling the base current to the NPN transistor. This transistor is biased as an emitter follower.

The structure of a memory cell embodying the invention to the contrary comprises a merged P channel

MOS and N channel MOS structure having a common gate electrode wherein by applying a positive (negative) potential to the gate electrode one (the other) of the channels is turned on while the other (one) channel is turned off.

Figure 4A shows another memory cell embodying the invention which relies on punch-through to charge the floating substrate corresponding to P type well 102 in Figure 1A and P type well 202 in Figure 2A. This memory cell has a vertical structure and consequently a memory array formed therewith will have a much smaller area per memory cell than the previously described array. Here the P+ type diffusion line corresponding to P+ type region 101 in Figure 1A and P+ type region 201 in Figure 2A becomes a buried region 407 formed within the semiconductor chip. Thus, as shown in Figure 4A, N type substrate 408 on which is formed N+ type contact region 406 to be used for controlling the voltage applied to the substrate has formed thereon a P+ type region 407 by well-known means such as either ion-implantation or diffusion. The formation of a region such as region 407 is well-known in standard bipolar semiconductor processing and thus its formation will not be described in detail. Following the formation of P+ type region 407, an N+ type layer 405 is formed on the top surface of substrate 408. This is followed then by the growth of N type epitaxial layer 404 in the substrate. During the growth of this epitaxial P+ type impurity formed in region 407 in the top surface of the substrate 408 partially diffuses out into epitaxial material 404. Following completion of the growth of epitaxial layer 404, a P type well 402 is diffused or otherwise formed in the top surface of epitaxial layer 404 and N+ type region 403 is then formed in P type well 402. The device is then oxidized and a gate oxide is formed over the intersection of a selected portion of P type well 402 with a top surface of the structure. Field oxide (not shown but corresponding to field oxide 150 in Figure 1A) is formed over the remainder of the device.

Note that the buried strip of P+ type diffusion 407 in cell 400 replaces the P+ type diffusion conductive strip 130, 230 or 330 of cells 100 (Figure 1A), 200 (Figure 2A) or 300 (Figure 3A), respectively. However in the memory cell shown in Figure 4A, the buried P+ type diffused region 407 is as shown in plan view of Figure 4B parallel to the X direction corresponding to conductive gate 111A or 111B rather than parallel to the Y direction as in the memory cells shown in Figures 1A and 2A and as exemplified by conductive strip 130 (Figure 1B). To write into the cell shown in Figure 4A, the P type well 402 must be negatively charged to OV or −3V as in the case of the memory cell shown in Figure 1A. The reading operation is also the same as for the memory cell of Figure 1A. Thus column read line Y(R) which is connected to a sense amplifier is precharged to a positive voltage and the change of voltage of the column read line Y(R) with gate 411 (X) turned on to about +5 volts is monitored. As with the memory cell of Figure 1A, a read operation is non-destructive, but unlike the memory cell of Figure 1A, a write operation is also non-destructive. Writing occurs only at the intersection of the selected column (Y(R)) and row (X(W)). Writing occurs through use of the well-known punch-thorugh mechanism (see, for example, U.S. Patent No. 3,648,127 entitled "Reach-through or Punch-through Breakdown for Gate Protection in MOS Devices" on an invention of Lenzinger for a brief explanation of the punch-through phenomenon). Punch-through occurs when the selected column Y(R) is at +5 volts and the selected row X(W) is at −2 volts or −5 volts but not when either one of these two is at zero volts and the other of these two is a 5 volts or there is any smaller difference in potential between the two. The junction depths, impurity concentrations and other dimensions of the memory cell shown diagrammatically in Figure 4A and in plan view in Figure 4B are so arranged that approximately 7 volts are required between N+ type region 403 (Y(R)), and P+ type region 407 (X(W)) to achieve punch-through. Therefore for any voltage greater than 7 volts, the potential of the P type well 402 will simply track the difference over 7 volts.

The correct sequence for writing information into P type well 402 is thus to first raise column read line Y(R) to +5 volts, then drop the voltage on row write line X(W) to −2 or −5 volts, bring read line Y(R) back to zero volts, and then bring write line X(W) back to zero volts. Although the substrate (406, 408, 405, 404 and 409) is at zero volts, the high resistivity N type epitaxial layer 404 (typically doped to a concentration of between 1×10^{14} and 1×10^{16} atoms cm^{-3}) means that the N type epitaxial region 409 in the punch-through region is virtually floating. Thus, when the P+ type 407 goes negative, the PN junction between P type well 402 and N type epitaxial layer 404 is forward biased charging the P type well 402 with electrons.

An isoplanar version of the memory cell shown in Figure 4A is shown in plan view in Figure 4C. Using isoplaner processing saves area and increasing the packing density available. As with the part of the memory array shown in plan view in Figure 2B, oxide surrounds P type well 402 on three sides while on the fourth side is substrate 404 to which N+ type region 403 is connected by a channel through P type well 402 when the proper potential is applied to gate electrode 411 during a read operation.

As a further means of reducing the size of an array of memory cells embodying the invention one gate 411 can be used for two adjacent P type wells 402 and the particular P type well to be read from can be controlled merely by selecting the proper column line Y(R) attached to N+ type region 403 for activation. As shown in Figure 4C the P type regions 402 in adjacent memory cells are formed asymmetrically to allow one gate structure 411 to control two adjacent P type wells.

An advantage of the memory cell shown in Figures 4A, 4B and 4C is that a memory array formed therefrom becomes very compact and employs natural isolation of the P type well 402. Furthermore, non-destructive readout can be employed with a large read signal and the memory cell is relatively insensitive to soft errors such as those generated by alpha particles. Finally, the memory cell array embodying the invention also has better storage time. Again, however, the processing is relatively more complicated involving the formation

of high conductivity, buried, diffused strips and a high resistivity epitaxial layer and tight control in diffusion processes. This consideration alone may require the buried strips to be formed of arsenic or antimony diffusions thereby dictating reversing polarities of all other diffusion regions shown in Figure 4A. The buried row X(W) line corresponding to region 407 will have a higher parasitic capacitance and therefore a slower write operation than prior art devices, but this structure is perhaps of particular use in an isolated substrate technology such as the silicon-on-sapphire technology. Finally, the dimensions of the device must be carefully controlled to insure that one can write information into a given cell without disturbing the adjacent cells.

The embodiments described above store information by virtue of the presence or absence of charge on their floating substrates corresponding to P type wells 102, 202, 302 and 402. Each memory cell has its own isolated substrate as well as its own source diffusion isolated from other such diffusions by the substrate diffusion or alternatively by a dielectric wall on three of its four sides. All the embodiments can be implemented in either N channel or P channel technologies with the basic process closely resembling single or double level polysilicon CMOS processes. The process can yield CMOS type devices in the periphery which can then be used to advantage for reducing the chip power dissipation and handling positive and negative voltage pulses.

The read operation for all the embodiments is non-destructive with dynamic amplification at each storage site (memory cell). It is possible to have multi-level storage at each memory cell at the expense of more complex sense amplifiers able to detect multi-current levels. Thus the floating substrate 102 (Figure 1A) potential can be chosen to be one of four voltages, for example 0, −1.0 volt, −2.0 volt, and −3.0 volt, to provide two bit storage per cell without increase in cell area. These voltage levels can all be generated internally on chip.

For binary storage, three voltage levels are required on chip. These levels can be zero, −5 volts and −5 volts or any two externally applied voltages such as zero and +5 volts which can be used internally to provide a third level in a manner well known in the semiconductor arts (such as by using passive signal-level-varying circuits of a well-known design, or by voltage multiplication on chip, or by charge pumping to form a negative voltage from a positive voltage).

Two modes of programming are possible either by MOS transistor action as exemplified by the memory cell shown in Figures 1A, 2A and 3A or by punch-through as exemplified by the memory cell of Figure 4A. In addtion, under certain write or read conditions, the floating substrate may be charged unintentionally through charge pumping where a capacitively coupled diode becomes momentarily forward biased. This condition must be minimized for all bias conditions experienced by each cell. One way of doing this is by assuring a proper ratio of coupling capacitances between the floating substrate and its source diffusion capacitance C1, its body (drain) junction capacitance C2 and its gate capacitance C3. These capacitances are shown schematically in Figure 5. Ideally, the voltage on the substrate at Z 106 (Figure 5) and on column line Y(R) 120 should never vary from a given fixed voltage by more than a few hundred millivolts because of this effect and the gate capacitance C3 should be made as small as possible so that when the voltage on the gate 111 goes from zero volts to +5 volts during a read operation, the floating P type substrate is not sufficiently coupled to forward bias it with respect to the surrounding N+ type regions. Another way to minimize this effect is to have the Y(R) and Z contacts biased so that the floaing substrate cannot become forward biased under any operating conditions. For example, for the cell 100 shown in Figure 1A, Z can be kept at +5 volts with Y(R) kept at +5 volts during standby, going up to approximately 3.2 volts during read when X goes to +5 volts.

The choice of ratios for C_1, C_2 and C_3 determines not only the sensitivity of the cell to spurious signals but also its ability to store excess charge, as well as memory array access times. A higher storage capacity is important because of the reduced need for refreshing, and because it increases the margin against potential alpha particle upset and similar soft errors. However, unlike prior art dynamic RAM cells, the sizes of the excess charge packet on the floating substrate can be made very small since it is not this charge that is detected during a read operation, but rather an amplified signal whose magnitude is determined by the threshold of the accessed MOS transistor (made up, for example, of regions 103, 102 and 104 in the structure of Figure 1A).

The choice of doping concentrations and oxide thicknesses determine not only the relative values of C_1, C_2 and C_3, but also the effectiveness of the body effect that is the relationship between the potential on the floating substrate relative to the source and the threshold voltage of the MOS transistor.

To a first order approximation, the potential V_F on the floating substrate can be described by the following equation

$$V_F = \frac{(C_1V_{Y(R)} + C_2V_Z + C_3V_X + Q_F)}{(C_1 + C_2 + C_3)}$$

where Q_F is the excess charge on the floating substrate (zero for the low threshold state "0", and negative for the higher threshold state "1").

For a typical device the magnitude of Q_F required to give a ΔV_F of three volts is:

$$Q_F = \Delta V_F . (C_1 + C_2 + C_3) = 3 \times 10^{-14} \text{ coulombs} \simeq 10^5 \text{ electrons.}$$

It is clear from the above discussion that the choice of read voltages depends on the choice of C_1, C_2, and C_3 with several different possibilities dictated by design and process considerations. The one single constraint is that no read condition should permit the floating substrate to become excessively forward biased, although foward biasing up to about one volt is permissible.

In the manufacture of the memory cell of Figure 2A, for example, each bit or cell is formed in an N- type substrate 204 on which has been formed thick isoplanar field isolation oxide 212, by forming a window 103 in a diffusion masking oxide and diffusing first a deep P type region 202 (the floating substrate in the to-be-formed N+PN P+ type structure made up of regions 203, 202, 204 and 201 respectively) then an N+ type source region 203 is driven less deeply into the structure than deep P type region 202. Region 202 is contacted by a N+ type doped line 220 comprising read column Y(R) and region 201 is contacted by a P+ type doped line 230 comprising write column Y(W). Preferably these lines are formed of polycrystalline silicon. The defined lines 220 and 230 are also used as a mask to etch away the diffusion masking oxide in exposed regions where channel regions 214 and 202 will be formed. A gate oxide 210 is grown which is also used to form isolation between lines 220, 230 and a second level interconnection 211(X) which runs perpendicular to lines 220 and 230 (see Figure 7). The second level interconnect 211(X) forms the X line and can be either polycrystalline silicone or a metal or a metal silicide interconnect structure. Contacts are made in the periphery of the chip to the N type subastrate (Z) and to the Y(R), Y(W) and X lines.

In cell 200 shown in Figures 2A and 2B, the isolation is formed by partial oxidation of the silicon surface in a manner such as that taught in U.S. Patent No. 3,648,125 which discloses the isoplanar process to form vertical oxide walls which restrict the side-way diffusion of the P-regions 202 in three out of four directions and thereby allow adjacent P type regions to be brought closer together than in the structure of Figure 1A. Other than this isolation, the basic structure and process for the formation of cell 200 is similar to that used in the formation of cell 100.

The table below illustrates the bias voltage ranges for the various operating modes of the dynamic RAM cells 100, 200, 300 and 400 disclosed in Figures 1A, 2A, 3A and 4A, respectively. The subscripts "sel" and "unsel" on the column headings denote either a selected or an unselected word line, write line or read line. Thus the notation "X_{sel} (V)" refers to the selected X word line, while the notation "X_{unsel} (V)" refers to the unselected X word lines. Similar meanings are attached to the corresponding subscripts on the other heading in the Table.

As pointed out in the Table, all sense amplifiers are activated to sense all the bits along an accessed row X prior to a write operation because writing into a given cell would destroy all information in the other cells along the same X line. Accordingly, the write operation includes two steps; (a) a read operation to read out and latch in a sense amplifier the information in the cells along the X word line; and (b) a write operation to place the data into the selected cell and to replace the previously read out data back into the other cells. The table illustrates the voltage levels typically contemplated for application to the various X and Y lines during these operations. Of interest, cell 400 is uniquely addressed for writing-in information by punch-through (cross point cell) at each cell. Therefore cell 400 can be read out a row at a time, if desired, but written into only a bit at a time without destroying the information in the other cells in the same row as the cell in which information is being written.

The voltages shown in the Table are only approximate and are intended to be relative not absolute. On-chip actual voltages may very well differ from those given in the table.

While the above invention has been described in conjunction with a substrate and diffused regions of selected conductivity types, the conductivity types can, of course, be reversed from those shown while still staying within the scope of the invention. In this situation, the read and write voltages would also be reversed in polarity. Where regions are described as formed by diffusion, they often can be formed using ion implantation, if desired.

Bias Voltage Ranges for Various Operating Modes of DRAM

Cells 100, 200, 300: Operation	X_{sel}(V)	X_{unsel}(V)	$Y(W)_{sel}$	$Y(W)_{unsel}$	$Y(R)_{sel}$	$Y(R)_{unsel}$	Z(V)
Read:	5	0	0	0	0 to 3V at S/A node	0 to 3V at S/A node	5V
Note: All sense amps are activated to sense all bits along an accessed row X							
Write 1 (High V_T)							
(a) Read:	5	0	0	0	0 to 3V	0 to 3V	5
(b) Write 1:	−5	0	−5 or −1.0, −2.0, −3.0V etc. for multi-level write	0 or −5V depending on data from (a)	0 to 3V	0 to 3V	5
Write 0 (Low V_T)							
(a) Read:	5	0	0	0	0 to 3V	0 to 3V	5
(b) Write:	−5	0	0	0 or −5V depending on data from (a)	0 to 3V	0 to 3V	5
Standby:	0	0	0	0	0 to 3V	0 to 3V	5

Cell 400: Operation	X_{sel}(V)	X_{unsel}(V)	$X(W)_{sel}$	$X(W)_{unsel}$	$Y(R)_{sel}$	$Y(R)_{unsel}$	Z(V)
Read:	5	0	0	0	0 to 3V at S/A node	0 to 3V at S/A node	5
Write 1 (High V_T):	0	0	−5	0	5	0	5
Write 0 (Low V_T):	0	0	−2.5	0	5	0	5

CLAIMS

1. A semiconductor memory cell comprising: a semiconductor substrate of a first conductivity type; a first region of a second conductivity type formed in said semiconductor substrate; a second region of said first conductivity type formed in said first region; a third region of said second conductivity type formed in said substrate spaced from said first region; means for applying selected potentials to said first, second and third regions and said substrate; and a conductive gate formed over, but insulated from, portions of said first region, said second region and said semiconductor substrate to enable a channel to be formed in said first region to connect said second region to said substrate.

2. A memory cell according to claim 1 and further comprising means for measuring the rate of change of voltage on said second region, said rate of change being a measure of the information stored in said first region.

3. A memory cell according to claim 1 or 2 and further comprising means for electrically applying selected potentials to said substrate, said second region and said third region to form a punch-through connection between said first and third regions to store a selected quantity of charge representative of information in said first region.

4. A semiconductor memory cell comprising: a semiconductor substrate of a first conductivity type; a first region of a second conductivity type formed in said semiconductor substrate; a second region of said first conductivity type formed in said first region; a third region of said second conductivity type formed in said substrate spaced from said first region; first insulation formed over the region between said second region and said third region; a conductive gate formed on said first insulation over said space between said second region and said third region to form a first transistor from said first region, and said third region and said substrate with a channel of said second conductivity type capable of being formed in said substrate and a second transistor from said second region, said substrate and said first region with a channel of said first conductivity type capable of being formed in said first region, said conductive gate comprising a common gate for both devices; and means applying selected potentials to said second and third regions, said conductive gate and said substrate to turn off one of said two transistors.

5. A memory cell according to claim 4 and further comprising: means for applying a first selected voltage to said conductive gate; means for applying a second selected voltage to said second region; means for applying a third selected voltage to said third region; and means for applying a fourth selected voltage to said substrate, said first, second, third and fourth voltages being selected to form a conductive channel between said first region and said third region to place a selected charge in said first region.

6. A memory cell according to claim 5, wherein said first, second, third and fourth voltages are selected to form a conductive channel through said first region from said second region to said substrate, the rate of change of voltage on said second region being a measure of the information stored in said first region.

7. A memory cell according to any preceding claim wherein said third region of said second conductivity type is formed in said substrate underneath said first region.

8. A memory cell according to any preceding claim, wherein a buried layer of said first conductivity type is formed in said substrate beneath said first region, said second region and said third region, said buried layer having a higher conductivity than said substrate.

9. A memory cell according to claim 8, and further comprising means for electrically contacting each region of said buried layer.

10. A memory cell according to claim 8 or 9 wherein oxidized portions of said substrate extend a selected distance through said substrate to define the lateral exent of portions of said first region, said second region and said third region.

11. A memory cell according to claim 10, wherein the oxidized portions of said substrate extend through said substrate to said buried layer to define the lateral extent of portions of said first region, said second region and said third region, and in conjunction with said buried layer, to electrically isolate said semiconductor structure from other semiconductor structures formed in the same chip of semiconductor material.

12. A memory cell according to any preceding claim, wherein said first region is of a lower conductivity than said third region.

13. A memory cell according to any preceding claim, wherein said semiconductor substrate of a first conductivity type is formed on a semiconductor support structure of the second conductivity type.

14. A memory cell according to any preceding claim, wherein said first conductivity type is N type conductivity and said second conductivity type is P type conductivity.

15. A memory cell according to any one of claims 1 to 13, wherein said first semiconductor type is P type conductivity and said second conductivity type is N type conductivity.

16. A semiconductor memory device comprising a plurality of cells and selected peripheral circuitry including sense amplifiers, formed in a semiconductor substrate of a first conductivity type, each cell comprising: a first region of a second conductivity type formed in said semiconductor substrate for the storage of charge representative of information; a second region of said first conductivity type formed in said first region; a third region of said second conductivity type formed in said substrate spaced from said first region; and meahs for forming a conductive path between said first region and said third region, to

control the charge stored in said first region in response to a first selected set of potentials applied to said substrate, said third region, said second region and said means for forming, and for forming a conductive channel from said second region to said substrate through said first region in response to a second selected set of potentials applied to said substrate, said third region, said second region and said means for forming, the rate of change of potential in said second region in response to said second set of potentials being indicative of the information stored in said first region.

17. A device according to claim 16 and further comprising: means for applying a first selected potential to said substrate; means for applying a second selected potential to said third region; means for applying a third selected potential to said second region; and means for applying a fourth selected potential to said means for forming, to change the information stored in said first region.

18. A device according to claim 16 or 17 wherein said means for forming comprises: insulation formed on the surface of the substrate, and gate electrode means formed over said insulation thereby to control the formation of a conductive channel across said first region from said second region to said substrate, thereby to enable the measurement of the state of the charge stored in said first region by measuring the rate of change of the voltage in said second region upon the application of a voltage to said gate electrode sufficient to form a channel across said first region, and to control the formation of conductive path between said first region and said third region thereby to place a selected charge in said first region so as to store selected information in said first region.

19. A device according to claim 16 and further comprising means for applying a selected potential to said gate electrode so as to form a channel between said first region and said third region, and means for controlling the potential applied to said third region so as to store a selected charge in said first region representaive of selected information.

20. A device according to claim 19, wherein said selected charge represents a selected one of several logic levels.

21. A device according to claim 19 or 12 wherein said selected charge represents a selected one of two logic levels.

22. A semiconductor memory cell substantially as hereinbefore described with reference to, and as illustrated in, the accompanying drawings.

23. A semiconductor memory device substantially as hereinbefore described with reference to the accompanying drawings.

24. Any novel feature or combination of features herein disclosed.

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