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(71) Applicant: **CELLINK CORPORATION** [US/US]; 610 Quarry Rd., San Carlos, California 94070 (US).

(72) Inventors: **TATE, Gabrielle**; 610 Quarry Rd., San Carlos, California 94070 (US). **ORTIZ, Jean-Paul**; 610 Quarry Rd., San Carlos, California 94070 (US). **FINDLAY, Will**; 610 Quarry Rd., San Carlos, California 94070 (US).

(74) Agent: **GUSEV, Vladimir Y.**; Polygon IP, LLP, 101 Jefferson Dr., Menlo Park, California 94025 (US).

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(54) Title: MULTILAYERED FLEXIBLE INTERCONNECT CIRCUITS FOR BATTERY ASSEMBLIES AND METHODS OF FABRICATING AND INSTALLING THEREOF

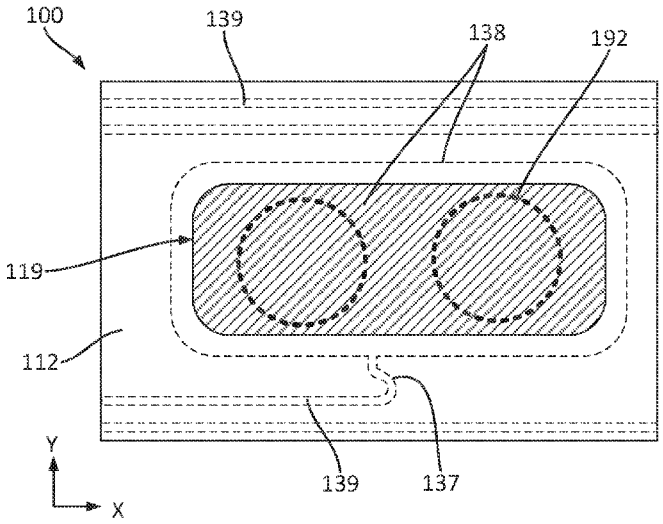

FIG. 1D

(57) **Abstract:** Provided are multilayered flexible interconnect circuits comprising multiple conductive layers. Also provided are methods of fabricating such circuits and also methods of fabricating battery assemblies with such circuits. A multilayered flexible interconnect circuit comprises at least two conductive layers and at least one inner insulator, which extends between these conductive layers in some circuit portions and allows for conductive layers to directly interface in other circuit portions (e.g., busbar portions). Outer insulators can be provided to insulate these conductive layers from the environment while allowing some access to these layers as needed. Each conductive layer and insulator can be individually patterned to achieve these functions. One or more insulators support conductive layers relative to each other as well as different portions (e.g., disjoined portions) of the same conductive layer. The same

WO 2025/106232 A1

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multilayered flexible interconnect circuit can provide battery interconnect, voltage/temperature sense, and/or other functions.

Multilayered Flexible Interconnect Circuits for Battery Assemblies and Methods of Fabricating and Installing Thereof

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit under 35 U.S.C. § 119(e) of US Provisional Patent Application 63/598,212 (Attorney Docket No. CLNKP026P) by Tate, et. al., entitled: "Multilayered Flexible Interconnect Circuits for Battery Assemblies and Methods of Fabricating and Installing Thereof", filed on 2023-11-13, which is incorporated herein by reference in its entirety for all purposes.

BACKGROUND

[0002] Battery cells in battery packs and other types of battery assemblies are typically interconnected using individual busbars. Each busbar is stamped from a sufficiently thick metal sheet (selected based on current ratings) and individually handled during the busbar installation (e.g., positioned over and welded to the battery terminals). Furthermore, additional circuits (e.g., voltage sense harnesses) can be installed and connected to these busbars during the battery pack fabrication. Overall, many different operations and components are used, which complicates the fabrication process.

[0003] What is needed are new circuit types, such as multilayered flexible interconnect circuits, that overcome various challenges associated with conventional busbars.

SUMMARY

[0004] Provided are multilayered flexible interconnect circuits comprising multiple conductive layers. Also provided are methods of fabricating such circuits and also methods of fabricating battery assemblies with such circuits. A multilayered flexible interconnect circuit comprises at least two conductive layers and at least one inner insulator, which extends between these conductive layers in some circuit portions and allows for conductive layers to

directly interface in other circuit portions (e.g., busbar portions). Outer insulators can be provided to insulate these conductive layers from the environment while allowing some access to these layers as needed. Each conductive layer and insulator can be individually patterned to achieve these functions. One or more insulators support conductive layers relative to each other as well as different portions (e.g., disjoined portions) of the same conductive layer. The same multilayered flexible interconnect circuit can provide battery interconnect, voltage/temperature sense, and/or other functions.

[0005] Clause 1. A multilayered flexible interconnect circuit comprising: a first outer insulator layer; a second outer insulator layer; an inner insulator layer; a first conductive layer; and a second conductive layer, wherein: the first outer insulator layer, the second outer insulator layer, the inner insulator layer, the first conductive layer, and the second conductive layer collectively define a busbar portion, a busbar support portion, an insulated conductor portion, and a metal-free portion of the flexible interconnect circuit, in the busbar portion, the first conductive layer and the second conductive layer directly interface with each other while a surface of the first conductive layer facing away from the second conductive layer is exposed, in the busbar support portion, the inner insulator layer is stacked between and directly interfaces each of the first conductive layer and the second conductive layer, in the busbar support portion, the first conductive layer is stacked between and directly interfaces the first outer insulator layer and the inner insulator layer, and in the busbar support portion, the second conductive layer is stacked between and directly interfaces the inner insulator layer and the second outer insulator layer.

[0006] Clause 2. The multilayered flexible interconnect circuit of clause 1, wherein, in the metal-free portion, the inner insulator layer is stacked between and directly interfaces the first outer insulator layer and the second outer insulator layer.

[0007] Clause 3. The multilayered flexible interconnect circuit of clause 2, wherein, in the insulated conductor portion: the second conductive layer is

stacked between and directly interfaces the inner insulator layer and the second outer insulator layer, and the inner insulator layer is stacked between and directly interfaces the second conductive layer and the first outer insulator layer.

[0008] Clause 4. The multilayered flexible interconnect circuit of clause 3, wherein the insulated conductor portion is positioned between the busbar support portion and metal-free portion.

[0009] Clause 5. The multilayered flexible interconnect circuit of clause 1, wherein the busbar support portion at least partially surrounds the busbar portion.

[0010] Clause 6. The multilayered flexible interconnect circuit of clause 1, wherein the busbar support portion is positioned between the busbar portion and the metal-free portion.

[0011] Clause 7. The multilayered flexible interconnect circuit of clause 1, wherein each of the first outer insulator layer, the second outer insulator layer, the inner insulator layer, the first conductive layer, and the second conductive layer is formed from a same starting sheet.

[0012] Clause 8. The multilayered flexible interconnect circuit of clause 1, wherein each of the first outer insulator layer, the second outer insulator layer, the inner insulator layer, the first conductive layer, and the second conductive layer has the same thickness and composition throughout an entire footprint of the flexible interconnect circuit.

[0013] Clause 9. The multilayered flexible interconnect circuit of clause 1, wherein each of the first outer insulator layer, the second outer insulator layer, and the inner insulator layer has an opening in the busbar portion.

[0014] Clause 10. The multilayered flexible interconnect circuit of clause 1, wherein: each of the first outer insulator layer and the second outer insulator layer comprises a polymer base and an adhesive layer covering a surface of and supported by the polymer base, the polymer base comprises one or more polymers selected from the group consisting of polyimide (PI), polyethylene

naphthalate (PEN), polyethylene terephthalate (PET), polymethyl methacrylate (PMMA), ethyl vinyl acetate (EVA), polyethylene (PE), polyvinyl fluoride (PVF), polyamide (PA), and/or polyvinyl butyral (PVB), and the adhesive layer comprises one or more of epoxy and polyurethane.

[0015] Clause 11. The multilayered flexible interconnect circuit of clause 10, wherein, in the busbar support portion: the adhesive layer of the first outer insulator layer directly interfaces and is adhered to the first conductive layer, and the adhesive layer of the second outer insulator layer directly interfaces and is adhered to the second conductive layer.

[0016] Clause 12. The multilayered flexible interconnect circuit of clause 1, wherein: the inner insulator layer comprises an inner polymer base, a first inner adhesive layer, and a second inner adhesive layer, the inner polymer base is positioned between and supports each of the first inner adhesive layer and the second inner adhesive layer, the inner polymer base comprises one or more polymers selected from the group consisting of polyimide (PI), polyethylene naphthalate (PEN), polyethylene terephthalate (PET), polymethyl methacrylate (PMMA), ethyl vinyl acetate (EVA), polyethylene (PE), polyvinyl fluoride (PVF), polyamide (PA), and/or polyvinyl butyral (PVB), and each of the first inner adhesive layer and the second inner adhesive layer comprises one or more of epoxy and polyurethane.

[0017] Clause 13. The multilayered flexible interconnect circuit of clause 12, wherein, in the busbar support portion: the first inner adhesive layer of the inner insulator layer directly interfaces and is adhered to the first conductive layer, and the adhesive layer of the second outer insulator layer directly interfaces and is adhered to the second conductive layer.

[0018] Clause 14. The multilayered flexible interconnect circuit of clause 1, wherein each of the first conductive layer and the second conductive layer comprises aluminum and has a thickness of 100-400 micrometers.

[0019] Clause 15. The multilayered flexible interconnect circuit of clause 1, further comprising a support unit adhered to the first outer insulator layer and

comprises a busbar access opening such that the busbar portion fully overlaps with the support unit.

[0020] Clause 16. The multilayered flexible interconnect circuit of clause 1, wherein the first outer insulator layer and second outer insulator layer comprise a set of flexibility slits in the metal-free portion surrounding the busbar support portion thereby providing out-of-plane flexibility of the busbar portion.

[0021] Clause 17. The multilayered flexible interconnect circuit of clause 1, further comprising a registration portion comprising: a first registration opening in the second outer insulator layer; and a second registration opening in the second conductive layer, wherein: a dimension of the first registration opening in a direction is larger than a dimension of the second registration opening in the same direction, the first registration opening and the second registration opening are aligned, a portion of the second conductive layer is visible through the first registration opening, and a portion of an insulator layer other than the second outer insulator layer is visible through the second registration opening.

[0022] Clause 18. The multilayered flexible interconnect circuit of clause 17, wherein the portion of an insulator layer other than the second outer insulator layer visible through the second registration opening is a portion of the inner insulator layer.

[0023] Clause 19. The multilayered flexible interconnect circuit of clause 1, further comprising at least one high-current conductor electrically unconnected with any of the busbars and comprising at least two conductive layers that directly interface one another.

[0024] Clause 20. The multilayered flexible interconnect circuit of clause 19, wherein the high-current conductor comprises at least one heatsink portion and at least one intersink portion, wherein: the heatsink portion and intersink portion are monolithic, the heatsink portion extends further in a width than the intersink portion, and a ratio of an extension of the heatsink portion in the width to an extension of the intersink portion in the same direction is at least 10:1.

[0025] Clause 21. A battery assembly comprising: a set of battery cells comprising cell terminals; and a multilayered flexible interconnect circuit comprising a first outer insulator layer, a second outer insulator layer, an inner insulator layer, a first conductive layer, and a second conductive layer, wherein: the first outer insulator layer, the second outer insulator layer, the inner insulator layer, the first conductive layer, and the second conductive layer collectively define a busbar portion, a busbar support portion, an insulated conductor portion, and a metal-free portion of the flexible interconnect circuit, in the busbar portion, the first conductive layer and the second conductive layer directly interface with each other, and both are welded to the cell terminals of two adjacent battery cells of the set of battery cells, in the busbar portion, a surface of the first conductive layer facing away from the second conductive layer interfaces with the cell terminals of the two adjacent battery cells of the set of battery cells, in the busbar support portion, the inner insulator layer is stacked between and directly interfaces the first conductive layer and the second conductive layer, in the busbar support portion, the first conductive layer is stacked between and directly interfaces the first outer insulator layer and the inner insulator layer, and in the busbar support portion, the second conductive layer is stacked between and directly interfaces the inner insulator layer and the second outer insulator layer.

[0026] Clause 22. The battery assembly of clause 21, wherein the busbar portion is positioned out of plane relative to other portions of the multilayered flexible interconnect circuit and closer to the cell terminals than the metal-free portion.

[0027] Clause 23. The battery assembly of clause 21, wherein in the busbar portion the first outer insulator layer comprises an opening that exposes the surface of the first conductive layer facing away from the second conductive layer.

[0028] Clause 24. The battery assembly of clause 23, wherein in the busbar portion the second outer insulator layer comprises an opening that exposes the

surface of the second conductive layer facing away from the first conductive layer.

[0029] Clause 25. The battery assembly of clause 21, wherein: the two battery cells are shifted out-of-plane relative to each other, and within the busbar portion the busbar is deflected out-of-plane relative to other portions of the multilayered flexible interconnect circuit and the welds are positioned out-of-plane relative to each other.

[0030] Clause 26. The battery assembly of clause 21, further comprising a vent-channel forming metal portion, wherein: the vent-channel forming metal portion is formed from one or both of the first conductive layer and the second conductive layer, the vent-channel forming metal portion is electrically unconnected to the busbars, and the vent-channel forming metal portion is positioned over and aligned with vent plugs of the battery cells.

[0031] Clause 27. The battery assembly of clause 26, wherein the vent-channel forming metal portion is a single monolithic strip.

[0032] Clause 28. The battery assembly of clause 26, wherein the vent-channel forming metal portion is patterned into multiple strips, thereby increasing an out-of-plane flexibility of the vent-channel forming metal portion.

[0033] Clause 29. The battery assembly of clause 21, wherein the multilayered flexible interconnect circuit further comprises a support unit adhered to the first outer insulator layer, wherein: the support unit comprises a busbar access opening such that the busbar portion fully overlaps with the busbar access opening, the support unit is positioned between the first outer insulator layer and battery cells, and the busbar is deflected out-of-plane relative to other portions of the multilayered flexible interconnect circuit and towards the cell terminals when the busbar is welded to the cell terminals.

[0034] Clause 30. The battery assembly of clause 29, wherein the support unit is bonded to the first outer insulator layer.

[0035] Clause 31. A method of fabricating a multilayered flexible interconnect circuit, the method comprising: laminating a first metal sheet to a first

temporary substrate; patterning the first metal sheet, while laminated to the first temporary substrate, thereby forming a first conductive layer; laminating a second metal sheet to a second temporary substrate; patterning the second metal sheet, while the laminated to the second temporary substrate, thereby forming a second conductive layer; and stack and laminate the first conductive layer, the second conductive layer, a first outer insulator layer, a second outer insulator layer, and an inner insulator layer thereby forming the flexible interconnect circuit, wherein: the multilayered flexible interconnect circuit is defined by a busbar portion, a busbar support portion, an insulated conductor portion, and a metal-free portion of the flexible interconnect circuit, in the busbar portion, the first conductive layer and the second conductive layer directly interface with each other while a surface of the first conductive layer facing away from the second conductive layer is exposed, in the busbar support portion, an inner insulator layer is stacked between and directly interfaces the first conductive layer and the second conductive layer, in the busbar support portion, the first conductive layer is stacked between and directly interfaces the first outer insulator layer and the inner insulator layer, and in the busbar support portion, the second conductive layer is stacked between and directly interfaces the inner insulator layer and the second outer insulator layer.

[0036] Clause 32. A method of fabricating a battery assembly, the method comprising: positioning a multilayered flexible interconnect circuit over a set of battery cells comprising cell terminals, wherein: the multilayered flexible interconnect circuit comprises a first outer insulator layer, a second outer insulator layer, an inner insulator layer, a first conductive layer, and a second conductive layer, the first outer insulator layer, the second outer insulator layer, the inner insulator layer, the first conductive layer, and the second conductive layer collectively define a busbar portion, a busbar support portion, an insulated conductor portion, and a metal-free portion of the flexible interconnect circuit, in the busbar portion, the first conductive layer and the second conductive layer directly interface with each other while a surface of the first conductive layer facing away from the second conductive layer is exposed, in the busbar support portion, the inner insulator layer is stacked

between and directly interfaces each of the first conductive layer and the second conductive layer, in the busbar support portion, the first conductive layer is stacked between and directly interfaces the first outer insulator layer and the inner insulator layer, and in the busbar support portion, the second conductive layer is stacked between and directly interfaces the inner insulator layer and the second outer insulator layer; pushing the busbar portion toward the cell terminals to establish a direct contact between the first conductive layer in the busbar portion and the cell terminals; and welding the first conductive layer in the busbar portion to the cell terminals.

[0037] Clause 33. The method of clause 32, wherein the multilayered flexible interconnect circuit further comprises at least one alignment feature thereby enabling the alignment of the multilayered flexible interconnect circuit with the battery cells such that the busbar portions of the multilayered flexible interconnect circuit are positioned over the cell terminals of the battery cells.

[0038] Clause 34. The method of clause 33, wherein the alignment feature comprises: a first registration opening in the second outer insulator layer; and a second registration opening in the second conductive layer, wherein: a dimension of the first registration opening in a direction is larger than a dimension of the second registration opening in the same direction, the first registration opening and the second registration opening are aligned, a portion of the second conductive layer is visible through the first registration opening, and a portion of an insulator layer other than the second outer insulator layer is visible through the second registration opening.

[0039] Clause 35. The method of clause 32, wherein during pushing of the busbar portion toward the cell terminals the busbar portion is deflected out-of-plane relative to other portions of the multilayered flexible interconnect circuit.

[0040] Clause 36. The method of clause 32, wherein when the first conductive layer is welded to the cell terminals, the second conductive layer in the busbar portion is also welded to the first conductive layer.

[0041] Clause 37. The method of clause 32, further comprising positioning a support unit between the first outer insulator layer and the battery cells prior to pushing the busbar portion toward the cell terminals.

[0042] Clause 38. The method of clause 37, further comprising bonding the support unit to the with an adhesive prior to pushing the busbar portion toward the cell terminals.

[0043] Clause 39. The method of clause 32, wherein the multilayered flexible interconnect circuit further comprises vent-channel forming metal portions formed from one or both of the first conductive layer and the second conductive layer and positioned over and aligned with vent plugs of the battery cells when the multilayered flexible interconnect circuit is positioned over the set of battery cells.

[0044] Clause 40. The method of clause 39, further comprising shaping the vent-channel forming metal portions to form a vent channel over the vent plugs after positioning the over the set of battery cells.

[0045] Clause 41. The method of clause 40, wherein: the vent-channel forming metal portions is formed by multiple strips, and one or both outer insulator layers has perforations, thereby increasing its out-of-plane flexibility.

[0046] These and other embodiments are described further below with reference to the figures.

BRIEF DESCRIPTION OF THE DRAWINGS

[0047] The included drawings are for illustrative purposes and serve only to provide examples of possible structures and operations for the disclosed inventive systems, apparatus, and methods. These drawings in no way limit any changes in form and detail that may be made by one skilled in the art without departing from the spirit and scope of the disclosed implementations.

[0048] FIG. 1A is a top view of a set of prismatic battery cells illustrating cell terminals and vent plugs of these cells, in accordance with some examples.

[0049] FIG. 1B is a top view of various conductive components of a multilayered flexible interconnect circuit used for interconnecting the prismatic battery cells of FIG. 1A as well as provide voltage sense functions, in accordance with some examples.

[0050] FIG. 1C is a top view of the entire multilayered flexible interconnect circuit comprising the conductive components of FIG. 1B and insulating layers (e.g., for supporting these conductive components) and used for interconnecting the prismatic battery cells of FIG. 1A, in accordance with some examples.

[0051] FIG. 1D is an expanded top view of a portion of the flexible interconnect circuit in FIG. 1C illustrates an opening in the top (second) outer insulator and various boundaries of the conductive components, in accordance with some examples.

[0052] FIG. 1E is a schematic side view of two battery cells interconnected by the busbar of a multilayered flexible interconnect circuit, in accordance with some examples.

[0053] FIG. 2A is a cross-sectional side view of a multilayered flexible interconnect circuit identifying various components and portions of the circuit, in accordance with some examples.

[0054] FIG. 2B is an expanded cross-sectional side view of the busbar support portion of the flexible interconnect circuit in FIG. 2A, in accordance with some examples.

[0055] FIGs. 2C-2E are other examples of the busbar support portion of a flexible interconnect circuit, in accordance with some examples.

[0056] FIG. 2F is a top expanded view of a portion of the flexible interconnect circuit that illustrates an opening in the top (second) outer insulator and various boundaries of the conductive components, in accordance with some examples.

[0057] FIGS. 2G and 2H are two different cross-sections at different locations (along the X-axis) of the flexible interconnect circuit in FIG. 2F, in accordance with some examples.

[0058] FIG. 3A is a top schematic view of a support unit of a flexible interconnect circuit, in accordance with some examples.

[0059] FIG. 3B is a top expanded view of a portion of the support unit in FIG. 3B with reference to various components of the battery cells, in accordance with some examples.

[0060] FIG. 3C is a side schematic view of a flexible interconnect circuit comprising a support unit prior to forming connections to battery cells, in accordance with some examples.

[0061] FIG. 3D is a side schematic view of the flexible interconnect circuit in FIG. 3E after forming the connections to the battery cells, in accordance with some examples.

[0062] FIG. 3E is a schematic perspective view of the flexible interconnect circuit in FIG. 3E illustrates insulator flexibility slits for enabling out-plane flexibility of the busbar portion, in accordance with some examples.

[0063] FIGS. 3F and 3G are two cross-sectional side views of the flexible interconnect circuit before and after forming the connection to a battery cell illustrating an out-of-plane flexibility provided by the flexibility slits in the outer insulators, in accordance with some examples.

[0064] FIGS. 4A and 4B are side schematic views of a flexible interconnect circuit comprising multiple conductive layers forming a busbar portion before and after forming connections to battery cells, in accordance with some examples.

[0065] FIG. 5A is a top schematic view of a portion of a flexible interconnect circuit illustrating an unconnected conductive layer portion extending over pressure release valves in battery cells, in accordance with some examples.

[0066] FIG. 5B is a side schematic view of the portion of the flexible interconnect circuit in FIG. 5A illustrates the unconnected conductive layer portion extending over the pressure release valves in the battery cells, in accordance with some examples.

[0067] FIGS. 5C and 5D are side schematic views of a portion of the flexible interconnect circuit in FIG. 5B before and after shaping the unconnected conductive layer, in accordance with some examples.

[0068] FIG. 5E is a top schematic view of a portion of a flexible interconnect circuit illustrating a registration portion, in accordance with some examples.

[0069] FIG. 5F is a schematic cross-sectional side view of the portion of a flexible interconnect circuit of FIG. 5E, in accordance with some examples.

[0070] FIG. 6A is a top schematic view of conductive layers of a flexible interconnect circuit illustrating a high-current conductor (e.g., a return busbar) positioned among busbars, in accordance with some examples.

[0071] FIG. 6B is a side cross-sectional view of the conductive layers of the flexible interconnect circuit in FIG. 6A, in accordance with some examples.

[0072] FIG. 6C is a side cross-sectional view of the conductive layers and corresponding insulating layers of the multilayered flexible interconnect circuit in FIGS. 6A and 6B, in accordance with some examples.

[0073] FIG. 6D is a top schematic view of conductive layers of a flexible interconnect circuit illustrating a high-current conductor (e.g., a return busbar) with integrated heatsink portions, in accordance with some examples.

[0074] FIGs. 6E and 6F are schematic cross-sectional side views of the portion of a flexible interconnect circuit shown in FIG. 6D, in accordance with some examples.

[0075] FIGS. 7A and 7B are schematic top and side views of a multilayered flexible interconnect circuit illustrating a capacitor being formed using two conductive layers and an inner insulator layer, extending between the two conductive layers, in accordance with some examples.

[0076] FIG. 8 is a process flowchart corresponding to a method of fabricating a multilayered flexible interconnect circuit, in accordance with some examples.

[0077] FIG. 9 is a process flowchart corresponding to a method of fabricating a battery pack using a multilayered flexible interconnect circuit, in accordance with some examples.

DETAILED DESCRIPTION

[0078] In the following description, numerous specific details are outlined to provide a thorough understanding of the presented concepts. In some examples, the presented concepts are practiced without some or all of these specific details. In other examples, well-known process operations have not been described in detail to unnecessarily obscure the described concepts. While some concepts will be described in conjunction with specific examples, it will be understood that these examples are not intended to be limiting.

[0079] Flexible interconnect circuits are used to deliver power and/or signals and are used for various applications, such as vehicles, appliances, electronics, and the like. One example of such flexible interconnect circuits is a harness. As noted above, a conventional harness uses a stranded set of small round wires. A separate polymer shell insulates each wire, adding to the size and weight of the harness. Unlike conventional harnesses, flexible interconnect circuits described herein have thin flat profiles, enabled by thin electrical conductors that can be positioned side-by-side. Each electrical conductor can have a flat rectangular profile. In some examples, electrical conductors (positioned next to each other) are formed from the same metal sheet (e.g., foil). For purposes of this disclosure, the term “interconnect” is used interchangeably with “flexible interconnect circuit”, the term “conductive layer” - with “conductor” or “conductor layer”, and the term “insulating layer “ – with “insulator”.

Introduction

[0080] As noted above, conventional busbars used for connecting battery cells are typically used as individual components stamped from thick metal sheets to ensure sufficient current capabilities. However, this individual component

aspect complicates the battery pack assembly process, e.g., requiring individual handling and alignment of each component. Furthermore, these thick metal sheets may not be sufficiently flexible to accommodate various alignment deviations among battery cells, which further complicates the installation process. Finally, various additional components (besides battery cells, e.g., voltage-sense harnesses) need to be connected to busbars adding even more operational complexities.

[0081] Multilayered flexible interconnect circuits described herein address various issues listed above. Specifically, a multilayered flexible interconnect circuit comprises at least two conductive layers and at least one inner insulator, which extends between these conductive layers in some circuit portions and allows for conductive layers to directly interface in other circuit portions (e.g., busbar portions). In other words, when high current-carrying capabilities are needed, multiple conductive layers (e.g., all conductive layers) are in that portion of the circuit. It should be noted that stacking multiple conductive layers increases the flexibility of this stack in comparison to a monolithic component with the same thickness (and the same current-carrying capability). Alternatively, when only low current-carrying capabilities are needed (e.g., for voltage sensing), fewer than all conductive layers (e.g., only one conductive layer) can be used in this circuit portion. Since all components of the same conductive layer are formed from the same initial metal sheet, these components may be monolithically integrated (and do not require any later connections). Furthermore, components of different conductive layers may directly interface with each other (e.g., through an opening within an inner insulator layer) and even welded to each other (e.g., through an opening within an outer insulator layer). In some examples, the components of different conductive layers may be welded to each other while welding these to various external components (e.g., battery terminals). It should be noted that one or more inner insulators allow stacking multiple conductive layers while forming electrical connections between these layers, e.g., having multiple voltage traces crossing over.

FIGS. 1A-1E: Examples of Multilayered Flexible Interconnect Circuit Assemblies

[0082] The functional and structural aspects of multilayered flexible interconnect circuits will now be described in the context of FIGS. 1A-1E. Specifically, FIG. 1A is a top view of prismatic battery cells 190 forming a set, in accordance with some examples. In the illustrated example, the set includes 32 battery cells arranged into a 4-by-8 grid. However, any other number and/or arrangements of battery cells are within the scope. Each battery cell 190 comprises cell terminals 192, such as a positive cell tab and a negative cell tab. In the illustrated example, both cell terminals 192 are positioned on the same side of battery cell 190. However, other examples (e.g., with cell terminals being positioned on opposite sides of battery cells 190) are also within the scope. In these examples, multiple multilayered flexible interconnect circuits may be used to interconnect the same set of battery cells 190. The cell terminals 192 are used for interconnecting the battery cells 190, e.g., with all cells being interconnected in series as further shown with the design of the multilayered flexible interconnect circuit 100 presented in FIGS. 1B and 1C. However, other connection schemes (e.g., parallel and various combinations of parallel and in-series connections) are also within the scope. Furthermore, FIG. 1A illustrates that each of the battery cells 190 comprises a vent plug 194 that allows for gases and other materials to escape from one or more battery cells 190 experiencing internal overpressurization (e.g., due to a thermal runaway). As further described below, a multilayered flexible interconnect circuit may be used to form vent channels above these vent plugs 194.

[0083] FIG. 1B is a top view of conductive components 130 of a multilayered flexible interconnect circuit 100 used for interconnecting the cell terminals 192 of the prismatic battery cells 190 in FIG. 1A, in accordance with some examples. Insulator layers are not shown in this view to better illustrate the footprint of these conductive components 130. Each conductive component is formed by one or more conductive layers. The number of the conductive layers forming

each component depends on the current carrying requirement of these specific components.

[0084] Specifically, these conductive components 130 may include busbars 138 and voltage traces 139. Busbars 138 are examples of high-current-carrying conductive components, each formed using multiple conductive layers of the multilayered flexible interconnect circuit 100. Busbars 138 are connected (e.g., welded) to the cell terminals 192 during the fabrication of a battery assembly 180 (e.g., a battery pack). It should be noted that during this fabrication operation, all busbars 138 are integrated and supported within the multilayered flexible interconnect circuit 100 thereby eliminating the need to handle and align each busbar (in comparison to conventional methods).

[0085] Voltage traces 139 are examples of low-current carrying conductive components, each formed using fewer than all conductive layers of the multilayered flexible interconnect circuit 100 (e.g., only one conductive layer for each voltage trace). However, having multiple conductive layers allows routing/stacking multiple voltage traces 139 in the same portion of the multilayered flexible interconnect circuit 100. Furthermore, precise patterning of each conductive layer allows the positioning of multiple voltage traces 139 side-by-side. Voltage traces 139 can be connected to each of the busbars 138 and some form of controller (e.g., a battery management system). More specifically, a voltage trace 139 can be monolithic with one or more busbars 138 or, more specifically, with a portion of the conductive layer that both forms this voltage trace 139 and a portion of the busbar. In some examples, a battery management system is a part of a multilayered flexible interconnect circuit 100. Alternatively, the busbar portion 102 can be connected to the multilayered flexible interconnect circuit 100 or, more specifically, to the voltage traces 139 of the multilayered flexible interconnect circuit 100 during the fabrication of a battery assembly 180 (e.g., a battery pack).

[0086] Overall, a multilayered flexible interconnect circuit 100 comprises multiple conductive layers stacked along the Z-direction as further described below with reference to FIGS. 2A-2E. Some conductive components 130 (e.g.,

high-current carrying components such as busbars 138) may be formed using all or at least two or more conductive layers. Other conductive components 130 (e.g., low-current carrying components such as voltage traces 139) may be formed using a single conductive layer or at least fewer than all conductive layers.

[0087] FIG. 1C is a top view of the flexible interconnect circuit 100 comprising the conductive components 130 of FIG. 1B and a second outer insulator layer 112 (which is a top insulator in this view), in accordance with some examples. Insulators (outer and inner insulator layers) are used to support the conductive components 130 within the multilayered flexible interconnect circuit 100. The support is particularly important with multiple conductive layers, disjoined components, extensions, and other features of conductive layers that may not be available in conventional circuits. As shown in FIG. 1C, the second outer insulator layer 112 comprises multiple openings 119, e.g., to expose at least portions of busbars 138 and, in some examples, vent plugs 194.

[0088] FIG. 1D is an expanded top view of a portion of the multilayered flexible interconnect circuit 100 in FIG. 1C illustrating openings 119 in the second outer insulator layer 112 and the boundaries of conductive components, in accordance with some examples. Specifically, a portion of the busbar 138 may overlap with the second outer insulator layer 112 (and, e.g., a first outer insulator layer 111 as shown in FIG. 1E) to support the busbar 138 within the multilayered flexible interconnect circuit 100. Furthermore, FIG. 1D illustrates a voltage trace 139 extending to the busbar 138 (and being monolithic with one of the conductive layers forming the busbar 138). A portion of the voltage trace 139 can be specifically shaped and referred to as a voltage trace connection portion 137. The voltage trace connection portion 137 may interconnect a linear portion of the voltage trace 139 and busbar 138 and allow for the out-plane movement of the busbar 138 relative to the linear portion of the voltage trace 139 while preserving this monolithic connection. FIG. 1D also illustrates additional voltage trace 139 extending next to each other (e.g., to other

busbars). As noted above, additional voltage traces can be offset along the Z-axis.

FIGS. 2A-2H: Examples of Different Portions of Multilayered Flexible Interconnect Circuits

[0089] FIG. 2A is a cross-sectional side view of multilayered flexible interconnect circuit 100, in accordance with some examples. The multilayered flexible interconnect circuit 100 illustrated in FIG. 2A comprises a first outer insulator layer 111, a second outer insulator layer 112, an inner insulator layer 141, a first conductive layer 131, and a second conductive layer 132. The first outer insulator layer 111, second outer insulator layer 112, inner insulator layer 141, first conductive layer 131, and second conductive layer 132 collectively define a busbar portion 102, a busbar support portion 104, and a metal-free portion 108 of the flexible interconnect circuit 100. In some examples, these components also define an insulated conductor portion 106 of the flexible interconnect circuit 100. The structure and function of each of these portions will now be described in more detail. These portions may have different combinations of the first outer insulator layer 111, second outer insulator layer 112, inner insulator layer 141, first conductive layer 131, and second conductive layer 132 thereby forming different components of the multilayered flexible interconnect circuit 100. For example, a combination of the busbar portion 102 and busbar support portion 104 forms a busbar 138. More specifically, the busbar portion 102 represents the exposed portion of the busbar 138 allowing various connections to the busbar. The busbar support portion 104 provides the mechanical support to the busbar portion 102.

[0090] Referring to FIG. 2A, in the busbar portion 102, the first conductive layer 131 and the second conductive layer 132 directly interface with each other. In other words, the inner insulator layer 141 is not a part of the busbar portion 102 or, more specifically, the inner insulator layer 141 has an opening that coincides with the busbar portion 102. The interfacing allows to directly

interconnect the first conductive layer 131 and the second conductive layer 132 (e.g., by welding).

[0091] Furthermore, the surface of the first conductive layer 131 facing away from the second conductive layer 132 is exposed, e.g., to form a direct connection to cell terminals 192. This exposure is provided by an opening in the first outer insulator layer 111. Similarly, the surface of the second conductive layer 132 facing away from the first conductive layer 131 is exposed, e.g., to allow for welding or other tools to reach the second conductive layer 132 such as while forming a connection to cell terminals 192. This exposure is provided by an opening in the second outer insulator layer 112. For example, in a battery assembly, the first conductive layer 131 may be positioned between the second conductive layer 132 and cell terminals 192. The welding of the first conductive layer 131 to the cell terminals 192 may be performed through the second conductive layer 132 such that this welding also interconnects the first conductive layer 131 and second conductive layer 132. Stacking and interconnecting the first conductive layer 131 and second conductive layer 132 allows a higher current between the cell terminals 192 connected to these conductive layers. In some examples, the busbar portion 102 provides a current rating of at least 50 Amperes, at least 100 Amperes, or even at least 200 Amperes. In the same or other examples, the collective thickness of all conductive layers forming the busbar portion 102 is at least 200 micrometers, at least 500 micrometers, at least 1 millimeter, or even at least 3 millimeters. This combined thickness depends on the (1) required current ratings, (2) one or more materials of the conductive layers, (3) the thickness of each layer, and (4) the number of layers. It should be noted that separating this thickness into multiple layers allows to provide flexibility in the busbar portion 102 as further described with reference to FIGS. 4A-4B. Furthermore, the multilayered design allows to use of different footprints/patterns for each conductive layer thereby monolithically integrating different features into one or more conductive layers.

[0092] To form a busbar portion 102, an opening is formed in each of the first outer insulator layer 111, second outer insulator layer 112, and inner insulator

layer 141. In other words, each of the first outer insulator layer 111, second outer insulator layer 112, and inner insulator layer 141 has an opening in the busbar portion 102. The opening in the inner insulator layer 141 allows the first conductive layer 131 and the second conductive layer 132 to directly interface with each other. The opening in the first outer insulator layer 111 provides access and exposes a portion of the first conductive layer 131, e.g., to form connections to cell terminals 192. The opening in the second outer insulator layer 112 provides access and exposes a portion of the second conductive layer 132, e.g., during welding of the second conductive layer 132 to the first conductive layer 131 and to the cell terminals 192.

[0093] Referring to FIG. 2A, in some examples, the busbar support portion 104 can partially surround and support the busbar portion 102. FIG. 2A is a schematic cross-sectional side view of a busbar support portion 104 of the multilayered flexible interconnect circuit 100, in accordance with some examples. Specifically, before being connected to cell terminal 192, different conductive layers are not interconnected or otherwise attached in the busbar portion 102. In other words, before being connected to cell terminals 192, the busbar portion 102 is a stack of multiple conductive layers that directly interface with each other but are not connected in the busbar portion 102. This connection is provided by the insulator layers in the busbar portion 102. Specifically, in the busbar support portion 104, the inner insulator layer 141 is stacked between and directly interfaces the first conductive layer 131 and the second conductive layer 132, e.g., as shown in FIGS. 2A and 2B. More specifically, the inner insulator layer 141 is bonded to and supports both the first conductive layer 131 and the second conductive layer 132. Furthermore, in the busbar support portion 104, the first conductive layer 131 is stacked between and directly interfaces the first outer insulator layer 111 and the inner insulator layer 141. The first conductive layer 131 can be bonded to and supported by both the first outer insulator layer 111 and the inner insulator layer 141. Finally, in the busbar support portion 104, the second conductive layer 132 is stacked between and directly interfaces the inner insulator layer 141 and the second outer insulator layer 112. Again, the second conductive

layer 132 can be bonded and supported by both the inner insulator layer 141 and the second outer insulator layer 112. Overall, all three of the inner insulator layer 141, the first outer insulator layer 111, and the second outer insulator layer 112 can be used to support the first conductive layer 131 and second conductive layer 132 relative to each other and other components in the multilayered flexible interconnect circuit 100, at least in the busbar support portion 104.

[0094] In some examples, at least one of the first outer insulator layer 111 or the second outer insulator layer 112 or even both the first outer insulator layer 111 and the second outer insulator layer 112 are not present in the busbar support portion 104 thereby exposing one or both of the first conductive layer 131 and second conductive layer 132. The support to the first conductive layer 131 and the second conductive layer 132 can be provided by at least the inner insulator layer 141.

[0095] In other examples, the inner insulator layer 141 is not present in the busbar support portion 104. FIG. 2C is a schematic cross-sectional side view of a busbar support portion 104 of multilayered flexible interconnect circuit 100, in accordance with some examples. In these examples, first conductive layer 131 directly interfaces second conductive layer 132. First outer insulator layer 111 is bonded to and supports first conductive layer 131. Second outer insulator layer 112 is bonded to and supports second conductive layer 132. In these examples, first outer insulator layer 111 and second outer insulator layer 112 together provide necessary support to the conductive layers.

[0096] As noted above, the multilayered flexible interconnect circuit 100 illustrated in FIG. 2A comprises at least two conductive layers, e.g., a first conductive layer 131 and a second conductive layer 132. However, any number of conductive layers are within the scope. FIG. 2D is a schematic cross-sectional side view of the busbar support portion 104 of a multilayered flexible interconnect circuit 100, in accordance with some examples. In the example of FIG. 2D, the multilayered flexible interconnect circuit 100 comprises a third conductive layer 133. In this example, the multilayered flexible interconnect

circuit 100 comprises two inner insulators. A second inner insulator 142 is positioned between the second conductive layer 132 and the third conductive layer 133. In some examples, a multilayered flexible interconnect circuit 100 comprises four, five, six, or even more conductive layers. In some other examples, one or more inner insulator layers is not present, and the entire support of the conductive layers is provided by first outer insulator layer 111 and second outer insulator layer 112. For example, FIG. 2E is a schematic cross-sectional side view of the busbar support portion 104 of a multilayered flexible interconnect circuit 100, in accordance with some examples. In the example illustrated in FIG. 2E, the multilayered flexible interconnect circuit 100 has in the busbar support portion 104 first conductive layer 131, second conductive layer 132, and third conductive layer 133. First outer insulator layer 111 directly interfaces first conductive layer 131 and second outer insulator layer 112 directly interfaces third conductive layer 133. First outer insulator layer 111 is bonded to and supports first conductive layer 131 and second outer insulator layer 112 is bonded to and supports third conductive layer 133. In this example, there are no inner insulator layers present in the busbar support portion 104.

[0097] Referring to FIG. 2A, in some examples, in the metal-free portion 108, the inner insulator layer 141 is stacked between and directly interfaces the first outer insulator layer 111 and the second outer insulator layer 112. The metal-free portion 108 may be used for supporting different insulators relative to each other in the multilayered flexible interconnect circuit 100. Alternatively, the metal-free portion 108 is formed by the first outer insulator layer 111 and the second outer insulator layer 112 but not by the inner insulator layer 141 (i.e., the inner insulator layer 141 may not extend through the metal-free portion 108). Furthermore, in some examples, the metal-free portion 108 may be formed by the inner insulator layer 141 and only one or the first outer insulator layer 111 and the second outer insulator layer 112. The metal-free portion 108 can form at least some of the outside edges of the multilayered flexible interconnect circuit 100 (e.g., to position and seal the first conductive layer 131 and second conductive layer 132 away from these edges). In some examples, all conductive layers of the multilayered flexible interconnect circuit

100 are positioned away from the edges of the multilayered flexible interconnect circuit 100. In this example, the connections to the conductive layers may be formed through various openings in the insulators. Alternatively, at least a portion of the first conductive layer 131 and/or second conductive layer 132 may extend through one or more edges of the multilayered flexible interconnect circuit 100.

[0098] Referring to FIG. 2A, in some examples, the multilayered flexible interconnect circuit 100 comprises an insulated conductor portion 106. Unlike the busbar support portion 104, which comprises multiple conductive layers (e.g., all conductive layers forming the adjacent the busbar portion 102), an insulated conductor portion 106 can include fewer than all conductive layers, such as only one conductive layer, e.g., a second conductive layer 132 as shown in FIG. 1A. Specifically, in the insulated conductor portion 106, the second conductive layer 132 is stacked between and directly interfaces the inner insulator layer 141 and the second outer insulator layer 112. The inner insulator layer 141 is stacked between and directly interfaces the second conductive layer 132 and the first outer insulator layer 111. Referring to FIG. 2A, in some examples, the insulated conductor portion 106 is positioned between the busbar support portion 104 and metal-free portion 108. In the same or other examples, the busbar support portion 104 is positioned between the busbar portion 102 and the metal-free portion 108.

[0099] In some examples, each of the first outer insulator layer 111, the second outer insulator layer 112, the inner insulator layer 141, the first conductive layer 131, and the second conductive layer 132 is formed from the same starting sheet. As such, each of the first outer insulator layer 111, the second outer insulator layer 112, the inner insulator layer 141, the first conductive layer 131, and the second conductive layer 132 may have the same thickness and composition throughout the entire footprint of the flexible interconnect circuit 100. In fact, some layers (e.g., the first outer insulator layer 111 and/or the second outer insulator layer 112) may be monolithic throughout the entire footprint of the flexible interconnect circuit 100. Other layers may be cut into

disjoined components, e.g., busbars, insulating patches, etc. It should be noted that each layer is individually patterned to form different portions/components of the multilayered flexible interconnect circuit 100.

[00100] Referring to FIG. 2B, in some examples, each of the first outer insulator layer 111 and the second outer insulator layer 112 comprises a polymer base and an adhesive layer covering a surface of and supported by the polymer base. The polymer base comprises one or more polymer selected from the group consisting of polyimide (PI), polyethylene naphthalate (PEN), polyethylene terephthalate (PET), polymethyl methacrylate (PMMA), ethyl vinyl acetate (EVA), polyethylene (PE), polyvinyl fluoride (PVF), polyamide (PA), and/or polyvinyl butyral (PVB). The adhesive layer comprises one or more of epoxy and polyurethane. In more specific examples, in the busbar support portion 104, the adhesive layer of the first outer insulator layer 111 directly interfaces and is adhered to the first conductive layer 131. The adhesive layer of the second outer insulator layer 112 directly interfaces and is adhered to the second conductive layer 132.

[00101] Referring to FIG. 2B, in some examples, the inner insulator layer 141 comprises an inner polymer base, a first inner adhesive layer, and a second inner adhesive layer. The inner polymer base is positioned between and supports each of the first inner adhesive layer and the second inner adhesive layer. The inner polymer base comprises one or more polymer selected from the group consisting of polyimide (PI), polyethylene naphthalate (PEN), polyethylene terephthalate (PET), polymethyl methacrylate (PMMA), ethyl vinyl acetate (EVA), polyethylene (PE), polyvinyl fluoride (PVF), polyamide (PA), and/or polyvinyl butyral (PVB). Each of the first inner adhesive layer and the second inner adhesive layer comprises one or more of epoxy and polyurethane. In more specific examples, in the busbar support portion 104, the first inner adhesive layer of the inner insulator layer 141 directly interfaces and is adhered to the first conductive layer 131. Furthermore, the adhesive layer of the second outer insulator layer 112 directly interfaces and is adhered to the second conductive layer 132.

[00102] In some examples, first outer insulator layer 111, second outer insulator layer 112, and inner insulator layer 141 are thermoformable. Thermoformable insulating layers provide the benefit of high aspect ratio coverage of the conductive layers. In these examples, first outer insulator layer 111. Second outer insulator layer 112, and inner insulator layer 141 may include (or be formed from) polyimide (PI), polyethylene naphthalate (PEN), polyethylene terephthalate (PET), polymethyl methacrylate (PMMA), ethyl vinyl acetate (EVA), polyethylene (PE), polyvinyl fluoride (PVF), polyamide (PA), and/or polyvinyl butyral (PVB).

[00103] In some examples, each of the first outer insulator layer 111 and second outer insulator layer 112 comprises polypropylene (PP). Polypropylene (PP) is relatively inexpensive compared to some other materials that may be used for insulating layers. This can lower the overall cost of materials to manufacture multilayered flexible interconnect circuit 100. However, polypropylene (PP) also has a relatively low surface energy compared with other materials. This low surface energy can make attaching other layers of the multilayered flexible interconnect circuit 100 to the first outer insulator layer 111 and/or the second outer insulator layer 112 challenging. In some examples, each of the first outer insulator layer 111 and the second outer insulator layer 112 further comprises a different polymer material having a higher surface energy, forming one or more outer sublayers directly interfacing the polypropylene (PP). For example, the one or more outer sublayers may comprise a polyurethane (PU), a polyamide (PA), polyethylene (PE), or polyethylene terephthalate (PET). In some examples, the one or more outer sublayers may comprise a non-conductive adhesive selected from the list comprising an epoxy, an acrylate, and a polyester.

[00104] In some examples, each of the first conductive layer 131 and the second conductive layer 132 comprises aluminum. However, other metals (e.g., copper) are also within the scope. In some examples, all conductive layers (e.g., both the first conductive layer 131 and the second conductive layer 132) are formed from the same material, e.g., aluminum, copper, or the like. Alternatively, different metals may be used for the first conductive layer 131

and the second conductive layer 132. The use of aluminum (instead of copper) may help with lowering the overall circuit weight and also with lowering the minimum achievable fuse current rating. Specifically, aluminum has a higher resistivity and lower melting temperature than copper. As such, forming fusible links in an aluminum conductive layer may allow for more precise control of the fusible parameters (for the same size tolerance). In general, the first conductive layer 131 and the second conductive layer 132 may be formed from any conductive material that is sufficiently conductive (e.g., a conductivity being greater than 10^6 S/m or even greater than 10^7 S/m to allow for current flow through the foil with low power loss.

[00105] In some examples, the first conductive layer 131 and the second conductive layer 132 may include a surface sublayer or coating for providing a low electrical contact resistance and/or improving corrosion resistance. The surface sublayer may assist with forming electrical interconnections using techniques/materials including, but not limited to, soldering, laser welding, resistance welding, ultrasonic welding, bonding with conductive adhesive, or mechanical pressure. Surface sublayers, which may provide a suitable surface for these connection methods include, but are not limited to, tin, lead, zinc, nickel, silver, palladium, platinum, gold, indium, tungsten, molybdenum, chrome, copper, alloys thereof, organic solderability preservative (OSP), or other electrically conductive materials. Furthermore, the surface sublayer may be sputtered, plated, cold-welded, or applied via other means. In some examples, the thickness of the surface sublayer may range from 0.05 micrometers to 10 micrometers or, more specifically, from 0.1 micrometers to 2.5 micrometers. Furthermore, in some examples, the addition of a coating of the OSP on top of the surface sublayer may help prevent the surface sublayer itself from oxidizing over time. The surface sublayer may be used when a base sublayer of the first conductive layer 131 and the second conductive layer 132 includes aluminum or its alloys. Without protection, exposed surfaces of aluminum tend to form a native oxide, which is insulating. The oxide readily forms in the presence of oxygen or moisture. To provide a long-term stable surface in this case, the surface sublayer may be resistant to the in-diffusion of

oxygen and/or moisture. For example, zinc, silver, tin, copper, nickel, chrome, or gold plating may be used as surface layers on an aluminum-containing base layer.

[00106] In some examples, each of the first conductive layer 131 and the second conductive layer 132 has a thickness of 100-400 micrometers or, more specifically, 200-300 micrometers. The total thickness of all conductive layers forming a busbar can be at least 400 micrometers, at least 600 micrometers, at least 800 micrometers, or even at least 1,000 micrometers such as 500-2,000 micrometers or, more specifically, 600-1,200 micrometers. This thickness depends on the current-carrying requirements from the busbar. In some examples, all conductive layers in a multilayered flexible interconnect circuit 100 have the same thickness, e.g., as shown in FIG. 2B. Alternatively, at least one conductive layer is thicker than another conductive layer in the multilayered flexible interconnect circuit 100, e.g., as shown in FIG. 2D (illustrating the first conductive layer 131 being thicker than the second conductive layer 132 and the third conductive layer 133).

[00107] Referring to FIG. 2B, in some examples, a multilayered flexible interconnect circuit 100 further comprises a circuit bonding layer 113, e.g., a double-sides pressure sensitive adhesive (PSA) layer.

[00108] FIGs. 2F-2H provide additional illustrations of various components positioned in different portions of the multilayered flexible interconnect circuit 100, in accordance with some examples. Specifically, FIG. 2G illustrates two voltage traces 139 (i.e., first voltage trace 139a and second voltage trace 139b) extending adjacent to a busbar 138 and stacked along the Z-axis. These two voltage traces 139 are isolated from each other by a second inner insulator 142. First voltage trace 139a may be formed from the third conductive layer 133, while the second voltage trace 139b may be formed from the second conductive layer 132. In fact, FIG. 2H illustrates the first voltage trace 139a being monolithic with a portion of the busbar 138, i.e., may be formed from the third conductive layer 133 extending across multiple different components.

FIGS. 3A-3G: Examples of Support Units and Flexibility Slits

[00109] Depending on the size of battery assemblies, the size/footprint of a multilayered flexible interconnect circuit 100 can be rather substantial. Handling a large-size flexible circuit can be challenging, in particular during the installation and alignment of the circuit relative to battery cells 190. In some examples, the rigidity of the multilayered flexible interconnect circuit 100 can be increased by incorporating a support unit 150 to the circuit. Specifically, the support unit 150 can be operable as an exoskeleton and provided in selected parts of the multilayered flexible interconnect circuit 100 where some additional mechanical support is needed.

[00110] FIG. 3A is a top schematic view of a support unit 150 of a multilayered flexible interconnect circuit 100, in accordance with some examples. Other components of the multilayered flexible interconnect circuit 100 are not shown in this figure. The purpose of a support unit 150 is to provide in-plane rigidity to other circuit components, such as a stack of a first outer insulator layer 111, first conductive layer 131, inner insulator layer 141, second conductive layer 132, and second outer insulator layer 112. Most of these layers are flexible and may change shape during fabrication, handling, and installation of the multilayered flexible interconnect circuit 100, which can cause various difficulties. As noted above, the stack may not be sufficiently rigid (at least to maintain the in-plane shape). Furthermore, as described above, in some examples, not all layers are present in various portions of the multilayered flexible interconnect circuit 100.

[00111] The support unit 150 may be formed from a rigid plastic material such as polypropylene, polystyrene, nylon, polycarbonate, and/or methacrylate. For example, a support unit 150 may be molded or 3-D printed. In some examples, support unit 150 may comprise various openings, such as busbar access openings 152 and vent channels 159. Referring to FIG. 3B, each busbar access opening 152 may be aligned with busbars 138 (and during the installation with cell terminals 192). These busbar access openings 152 may be similar to (e.g., overlap with) the openings in the first outer insulator layer 111,

the inner insulator layer 141, and the second outer insulator layer 112. In some examples, the busbar access openings 152 fully overlap with the openings in the first outer insulator layer 111, the inner insulator layer 141, and the second outer insulator layer 112. During the installation of the multilayered flexible interconnect circuit 100, the vent channels 159 may overlap with vent plugs 194 such that any gases escaping through these vent plugs 194 can flow through the vent channels 159 to the edges of the battery assembly 180.

[00112] Referring to FIGS. 3C and 3D, in some examples, the support unit 150 is positioned between the first outer insulator layer 111 and battery cells 190 during the installation of the multilayered flexible interconnect circuit 100. Prior to the installation, the support unit 150 may be bonded to the first outer insulator layer 111, e.g., using an adhesive. FIG. 3C is a side schematic view of the circuit comprising a support unit 150 prior to forming connections to battery cells 190, while FIG. 3D is a similar side schematic view of the same circuit after forming the connections to the battery cells 190. It should be noted that the busbar 138 is pushed out of the plane (along the Z-axis) while the remainder of the multilayered flexible interconnect circuit 100 is positioned at the same level.

[00113] FIG. 3E is a schematic perspective view of the flexible interconnect circuit in FIG. 3D illustrating insulator flexibility slits 114 for enabling out-plane flexibility of the busbar portion, in accordance with some examples. Specifically, the first outer insulator layer 111 and the second outer insulator layer 112 comprise a set of flexibility slits 114 in the metal-free portion 108 surrounding the busbar support portion 104 thereby providing out-of-plane flexibility of the busbar portion 102. These slits may be positioned around the corners of each busbar 138 and, in more specific examples, along the short edges of each busbar 138. Each slit may be disjoined from other slits to ensure that the first outer insulator layer 111 and the second outer insulator layer 112 can still provide support to other circuit components, e.g., the busbar.

[00114] FIGS. 3F and 3G are two cross-sectional side views of a multilayered flexible interconnect circuit 100 before and after forming the

connection to a battery cell 190 illustrating the out-of-plane flexibility provided by the flexibility slits 114 in the two outer insulators, in accordance with some examples. Furthermore, FIGS. 3E-3G illustrate the position of the flexibility slits 114 relative to the edge of the busbar 138 as well as relative to the support unit 150.

FIGS. 4A-4B: Out-of-plane Flexibility of Multiple Conductive Layers Forming Busbar Portions

[00115] FIGS. 4A and 4B are side schematic views of a multilayered flexible interconnect circuit 100 comprising multiple conductive layers forming a busbar 138 before and after forming connections to battery cells 190, in accordance with some examples. Specifically, in these illustrations, the two battery cells 190 are shifted out-of-plane (along the Z-axis) relative to each other. The multilayered nature of the busbar 138 provides improved out-of-plane flexibility in comparison to a solid busbar that has the same thickness (without sacrificing the current-carrying capabilities). It should be noted that different conductive layers of the busbar 138 are not interconnected, at least within the busbar portion 102. This lack of connection improves the flexibility/conformality of the busbar 138 prior to welding.

[00116] Once the multilayered flexible interconnect circuit 100 is installed and the busbar 138 is welded to the cell terminals 192, the flexibility is reduced as the different conductive layers of the busbar 138 are now interconnected. At this point (after the installation and forming the connection), the busbar flexibility is not desirable to preserve the electrical connections between the busbar 138 and the cell terminals 192.

FIGS. 5A-5F: Examples of Utilizing Unconnected Conductive Layer Portion

[00117] When conductive layers of a multilayered flexible interconnect circuit 100 are patterned (e.g., starting with a continuous metal sheet), some portions of this metal sheet might not be needed to form various conductive

components 130 such as busbars 138 and voltage traces 139. In some examples, the portions of the metal sheet that do not form any conductive components 130 can be removed (e.g., etched/cut/ablated away). This removal reduces the weight of the multilayered flexible interconnect circuit 100. Alternatively, some of these portions may be retained in a multilayered flexible interconnect circuit 100 to form other non-electrical components such as vent-channel forming metal portions 135.

[00118] FIG. 5A is a top schematic view of a portion of a multilayered flexible interconnect circuit 100 illustrating vent-channel forming metal portions 135 extending over the vent plug 194 in battery cells 190, in accordance with some examples. These vent-channel forming metal portions 135 can be electrically unconnected to other conductive components 130, e.g., busbars 138. This electrical isolation/separation allows putting these vent-channel forming metal portions 135 in contact with various components, such as the case of the battery cell 190 as further described below with reference to FIG. 5D.

[00119] In some examples, vent-channel forming metal portion 135 can be a single monolithic strip. Alternatively, the vent-channel forming metal portion 135 can be patterned into multiple strips, e.g., to increase its out-plane flexibility/deformability as will now be described with reference to FIGS. 5B-5D. Specifically, FIG. 5B is a side schematic view of the portion of a multilayered flexible interconnect circuit 100 in FIG. 5A during the initial stages of the circuit installation over the battery cells 190. In this view, the busbar 138 is positioned over and aligned with the cell terminals 192, while the vent-channel forming metal portions 135 is positioned over and aligned with the vent plugs 194. FIG. 5C is a side schematic view of the portion of the multilayered flexible interconnect circuit 100 in FIG. 5B prior to shaping the vent-channel forming metal portion 135, in accordance with some examples. In this example, the vent-channel forming metal portion 135 is formed by multiple strips. Furthermore, one or both outer insulator layers (e.g., the second outer insulator layer 112) may have perforations to increase the out-of-plane

flexibility. FIG. 5D is a side schematic view of the same vent-channel forming metal portion 135 as in FIG. 5C after shaping this vent-channel forming metal portion 135 to form a vent channel 182 over the vent plugs 194.

[00120] Some portions of the metal sheet that do not form any conductive components 130 may be retained in a multilayered flexible interconnect circuit 100 to form registration portions 505. Such registration portions 505 may be beneficial as alignment features, for example, in aligning the multilayered flexible interconnect circuit 100 in the X-Y plane during manufacturing steps or installation. Such registration portions 505 may be formed, for example, during patterning of the insulating layers and conductive layers. In this way, forming registration portions 505 may provide a benefit in manufacturing time and cost as compared with, for example, creating registration marks by printing, painting, or etching marks or barcodes on an insulating layer outer surface in a separate manufacturing step. FIG. 5E is a top schematic view of a portion of a multilayered flexible interconnect circuit 100 illustrating a registration portion 505, in accordance with some examples. In some examples, registration portions 505 are formed from aligned openings in, for example, the second outer insulator layer 112 and the second conductive layer 132. In the example of FIG. 5E, first registration opening 510 is an opening, having a square shape, in second outer insulator layer 112. Aligned with first registration opening 510 is second registration opening 515. Second registration opening 515 is an opening, having a circle shape, in the second conductive layer 132. It should be noted that the length of the square shape of the first registration opening 510 along the line A-A is larger than the diameter of the circle shape of second registration opening 515 along the same line. In this way, the second registration opening 515 is visible through the first registration opening 510. FIG. 5F is a schematic cross-sectional side view of the multilayered flexible interconnect circuit 100 of FIG. 5E along line A-A, in accordance with some examples. As illustrated in FIG. 5F, a portion of inner insulator layer 141 is exposed through second registration opening 515 and first registration opening 510. In addition, a portion of second conductive layer 132 is exposed through the first registration opening 510. The appearance, when viewed as in the top

view of FIG. 5E, of a portion of inner insulator layer 141 surrounded by a portion of second conductive layer 132, in turn surrounded by second outer insulator layer 112, forms a high-contrast image. Also illustrated in FIG. 5F is a retained portion of first conductive layer 131 and a first outer insulator layer 111 intact where it contacts the retained portion of first conductive layer 131. In this way, the registration portion 505 does not require a through-hole extending entirely through the thickness of the multilayered flexible interconnect circuit 100. Other shapes are within scope for both the first registration opening 510 and the second registration opening 515, including, but not limited to, triangles, rectangles, pentagons, hexagons, stars, lozenges, and trapezoids. In some examples, a registration portion 505 comprises additional registration openings, for example, in additional insulator layers and/or additional conductive layers. In some examples, a registration portion 505 comprises openings in at least the first outer insulator layer 111 and the first conductive layer 131 and the registration portion 505 is visible from a bottom view of the multilayered flexible interconnect circuit 100.

FIGS. 6A-6F: Examples of Integrated Return Busbars

[00121] The patterning of continuous metal sheets allows forming of conductive components 130 that are positioned close to each other. Furthermore, with multiple conductive layers, different numbers of these layers may be used depending on the current-carrying requirements. These multilayered and patterning aspects allow the integrating of various features into a multilayered flexible interconnect circuit 100 such as voltage traces 139, described above. Furthermore, these aspects also allow integrating various high-current conductors 136, such as return busbars, as will now be described with reference to FIGS. 6A-6C. Specifically, FIG. 6A is a top schematic view of conductive layers of a flexible interconnect circuit illustrating a high-current conductor 136 (e.g., a return busbar) positioned among busbars 138, in accordance with some examples. The high-current conductor 136 is positioned proximate but unconnected to the busbars 138. To increase the current-

carrying capabilities of the high-current conductor 136, the high-current conductor 136 can be branched out into multiple lines (e.g., based on the spacing available between the busbar 138). It should be noted that despite all these branching, various parts of the high-current conductor 136 remain monolithically integrated. FIGS. 6B is a side cross-sectional view of the conductive layers of the flexible interconnect circuit in FIG. 6A, in accordance with some examples. FIG. 6C is a side cross-sectional view of the conductive layers and corresponding insulating layers of the multilayered flexible interconnect circuit in FIGS. 6A and 6B, in accordance with some examples.

[00122] In some examples, the multilayered and patterning aspects allow the integration of heat sinking features into the high-current conductor 136. FIG. 6D is a top schematic view of conductive layers of a portion of a multilayered flexible interconnect circuit 100, in accordance with some examples. As illustrated in FIG. 6D, high-current conductor 136 heatsink portions 604 and intersink portions 605 are proximate but unconnected to the busbars 138. The heatsink portions 604 and and intersink portions 605 are monolithic. The heatsink portions 604 extend further along the width than the intersink portions 605 without contacting any of the busbars 138. For example, the ratio of the extension of the heatsink portions 604 along the width to the extension of the intersink portions 605 in the same direction may be at least 2:1, at least 5:1, at least 10:1, at least 25:1, at least 50:1, or even at least 100:1.

[00123] The heatsink portion 604 and intersink portion 605 both transfer electric current. Specifically, the heatsink portion 604 transfers an electric current I_A and the intersink portion 605 transfers an electric current I_B, and I_A and I_B are equal. FIG. 6E is a schematic cross-sectional side view of multilayered flexible interconnect circuit 100, along line A-A of FIG. 6D. In FIG. 6E, high-current conductor 136 and busbar 138 are both shown. FIG. 6F is a schematic cross-sectional side view of multilayered flexible interconnect circuit 100, along line B-B of FIG. 6D. In FIG. 6F, no busbar 138 is included. As shown in FIG. 6E, the cross-section of high-current conductor 136 in the intersink portion 605 is smaller than its cross-section in heatsink portion 604, as shown in FIG. 6F. The

electrical resistance of the high-current conductor 136 is higher in the intersink portion 605 than in the heatsink portion 604. Returning to FIG. 6D, the current density, J_B, and the resistive heat generated by the transfer of electric current is also higher in intersink portion 605 than the current density, J_A, and resistive heat generated in heatsink portion 604. The high thermal conductivity of the metal of the high-current conductor 136 allows heat generated in the intersink portion 605 to flow to the heatsink portion 604. The higher surface area to volume ratio of the heatsink portion 604 allows the heat to more readily radiate from the heatsink portion 604 than from the intersink portion 605. In this way, the heatsink portion 604 allows the high-current conductor 136 to transfer higher electrical currents than would be possible by a high-current conductor 136 lacking a heatsink portion 604. As illustrated in FIG. 6D, the multilayered flexible interconnect circuit 100 may comprise multiple heatsink portions 604.

FIGS. 7A-7B: Examples of Integrated Capacitors

[00124] FIGS. 7A and 7B are schematic top and side views of a multilayered flexible interconnect circuit 100 illustrating an integrated capacitor 128 being formed using two conductive layers (e.g., a first conductive layer 131 and a second conductive layer 132) and an inner insulator layer 141, extending between the two conductive layers, in accordance with some examples. Similar to vent-channel forming metal portions 135 and high-current conductors 136 described above, an integrated capacitor 128 is formed from otherwise available conductive layer portions (e.g., portions not used to form any other conductive components 130), which may be referred to as “dead metal islands”. The electrical connection of the dead metal islands in parallel with sensitive components can provide a degree of electrostatic discharge (ESD) protection to these components.

FIG. 8: Examples of Methods of Fabricating Flexible Interconnect Circuits

[00125] FIG. 8 is a process flowchart corresponding to method 800 of fabricating a flexible interconnect circuit 100, in accordance with some examples. Various examples and features of multilayered flexible interconnect circuits 100 are described above. Specifically, a multilayered flexible interconnect circuit 100 comprises at least two conductive layers, e.g., a first conductive layer 131 and a second conductive layer 132. These conductive layers can have different patterns to provide various features described above. Furthermore, the multilayered flexible interconnect circuit 100 also comprises a first outer insulator layer 111, a second outer insulator layer 112, and an inner insulator layer 141 that is used to support and, in some parts, to insulate the first conductive layer 131 and the second conductive layer 132.

[00126] Method 800 may comprise (block 810) patterning each conductive layer and, separately, (block 820) patterning each insulator layer. In fact, each layer of a multilayered flexible interconnect circuit 100 can be patterned individually prior to laminating these layers together. In some examples, various temporary substrates may be used for these patterning operations. A temporary substrate can be used to support the patterned layer during and after the patterning operation. The temporary substrate is removed when the patterned layers are stacked.

[00127] As such, in some examples, method 800 or, more specifically, (block 810) patterning each conductive layer comprises (block 812) laminating a first metal sheet to a first temporary substrate and (block 814) patterning the first metal sheet, while the first metal sheet remains laminated on the first temporary substrate thereby forming a first conductive layer 131. For example, initially, the metal sheet may be a continuous self-supporting metal foil that can be processed and handled without any additional support. The pattern of the first conductive layer 131 may include disjoined components (e.g., busbar portions), narrow conductive traces, and/or other features that can be self-supported. Unlike, the first conductive layer 131, the temporary substrate is not patterned (e.g., the temporary substrate may remain as a continuous sheet). In some examples, the same temporary substrate may support multiple instances

of first conductive layers 131 (e.g., used for the production of multiple units of multilayered flexible interconnect circuits 100). Various patterning techniques are within the scope. For example, conductive layers can be patterned using chemical etching, mechanical cutting, laser cutting, and the like.

[00128] Similarly, method 800 or, more specifically, (block 810) patterning each conductive layer comprises (block 816) laminating a second metal sheet to a second temporary substrate and (block 818) patterning the second metal sheet to a second temporary substrate thereby forming a second conductive layer 132. It should be noted that the pattern of the first conductive layer 131 is different from the pattern of the second conductive layer 132. For example, a busbar (formed by both conductive layers) may have only one conductive layer protruding away and forming a voltage trace.

[00129] Method 800 may also comprise (block 820) patterning one or more insulator layers to form various openings. These openings (in the outer insulator layers) are used to provide access to the conductive layers at some locations (e.g., busbars). Furthermore, the openings in inner insulator layers allow the interconnection of the conductive layers at some locations (e.g., busbars). In some examples, after patterning insulator layers, at least one insulator represents a continuous structure (that is able to self-support and does not require any additional structures).

[00130] Method 800 further comprises (block 830) stacking and laminating the first conductive layer 131, second conductive layer 132, first outer insulator layer 111, second outer insulator layer 112, and inner insulator layer 141 thereby forming a flexible interconnect circuit 100. In some examples, this stacking and laminating operation comprises (block 834) laminating the first conductive layer 131 to a first outer insulator layer 111 and/or inner insulator layer 141 and removing any temporary support from the first conductive layer 131. After laminating to one or both of the insulator layers, the first conductive layer 131 is supported by one or both of the insulator layers and the temporary support is no longer needed. Similarly, the second conductive layer 132 may be laminated to a second outer insulator layer 112

and/or inner insulator layer 141 and remove any temporary support from the second conductive layer 132. A combination of a patterned conductive layer (e.g., a first conductive layer 131, a second conductive layer 132) and one or two insulators laminated to this patterned conductive layer may be referred to as a metal-insulator unit. Forming these insulator units prior to forming a full stack of the multilayered flexible interconnect circuit 100 allows the removal of any temporary substrates. Method 800 then proceeds with (block 838) stacking and laminating these metal-insulator units, each comprising at least one patterned conductive layer. In some examples, a patterned conductive layer comprises two patterned conductive layers, e.g., an inner insulator layer 141 with a first conductive layer 131 laminated to one side and a second conductive layer 132 laminated to the other side.

[00131] In some examples, method 800 comprises (block 840) attaching a support unit 150, e.g., to a first outer insulator layer 111. For example, a support unit 150 may have an adhesive layer interfacing the first outer insulator layer 111 during this operation. Additional features of the support unit 150 are described above.

FIG. 9: Examples of Methods of Fabricating Battery Assemblies Comprising Flexible Interconnect Circuits

[00132] FIG. 9 is a process flowchart corresponding to method 900 of fabricating a battery assembly 180, in accordance with some examples. A battery assembly 180 may be also referred to as a battery module or a battery pack and comprises multiple battery cells 190 and a multilayered flexible interconnect circuit 100 interconnecting these battery cells 190 and, in some examples, providing additional functionality (e.g., voltage traces, vent channels, and the like).

[00133] Method 900 comprises (block 910) positioning a multilayered flexible interconnect circuit 100 over a set of battery cells 190. As shown in FIG. 1A, the battery cells 190 comprise cell terminals 192. The busbar portions 102 of the multilayered flexible interconnect circuit 100 are positioned over the cell

terminals 192 during this operation. Various alignment features can be provided on the multilayered flexible interconnect circuit 100 to enable this operation. In some examples, a battery-facing component of the multilayered flexible interconnect circuit 100 (e.g., a support unit 150 or a first outer insulator layer 91) is also bonded to the battery cells 190 (e.g., using an adhesive layer such as a double-sided PSA).

[00134] Method 900 proceeds with (block 920) pushing the busbar portion 102 toward the cell terminals 192 to establish direct contact between the busbar portion 102 (or, more specifically, the first conductive layer 131 of the busbar portion 102) and the cell terminals 192. In some examples, this pushing operation requires a substantial out-of-plane deflection of the busbar portion 102 relative to other portions of the multilayered flexible interconnect circuit 100. Various features of the busbar support portion 104 enable this out-of-plane deflection as further described above.

[00135] Method 900 proceeds with (block 930) welding the busbar portion 102 to the cell terminals 192, e.g., using laser welding. However, other welding techniques are within the scope. It should be noted that when the busbar portion 102 to the cell terminal 192, all conductive layers forming the busbar portion 102 are also welded to each other.

Examples of Battery Assemblies with Multilayered Flexible Interconnect Circuits

[00136] FIGS. 1E as well as other figures discussed above illustrate some examples and aspects of a battery assembly 180 fabricated using a multilayered flexible interconnect circuit 100. In some examples, a battery assembly 180 comprises battery cells 190 (e.g., forming a set of battery cells) comprising cell terminals 192 and a multilayered flexible interconnect circuit 100 comprising a first outer insulator layer 111, a second outer insulator layer 112, an inner insulator layer 141, a first conductive layer 131, and a second conductive layer 132. Various examples of the multilayered flexible interconnect circuit 100 are described above. Specifically, the first outer insulator layer 111, the second

outer insulator layer 112, the inner insulator layer 141, the first conductive layer 131, and the second conductive layer 132 collectively define a busbar portion 102, a busbar support portion 104, an insulated conductor portion 106, and a metal-free portion 108 of the flexible interconnect circuit 100.

[00137] In the busbar portion 102, the first conductive layer 131 and the second conductive layer 132 directly interface with each other, and both are welded to the cell terminals 192 of two adjacent battery cells of the battery cells 190. Furthermore, in the busbar portion 102, a surface of the first conductive layer 131 facing away from the second conductive layer 132 interfaces with the cell terminals 192 of the two adjacent battery cells of the battery cells 190.

[00138] In the busbar support portion 104, the inner insulator layer 141 is stacked between and directly interfaces with each of the first conductive layer 131 and the second conductive layer 132. Furthermore, in the busbar support portion 104, the first conductive layer 131 is stacked between and directly interfaces the first outer insulator layer 111 and the inner insulator layer 141. Finally, in the busbar support portion 104, the second conductive layer 132 is stacked between and directly interfaces the inner insulator layer 141 and the second outer insulator layer 112.

[00139] In some examples, the busbar portion 102 is positioned out-of-plane and closer to the cell terminals 192 than the metal-free portion 108.

Conclusion

[00140] It is to be understood that the above description is intended to be illustrative, and not restrictive. For example, the above-described examples (and/or aspects thereof) may be used in combination with each other. In addition, many modifications may be made to adapt a particular situation or material to the teachings presented herein. Dimensions, types of materials, orientations of the various components, and the number and positions of the various components described herein are intended to define parameters of

some examples and are by no means limiting and are merely examples. Many examples and modifications within the spirit and scope of the claims will be apparent to those of skill in the art upon reviewing the above description.

CLAIMS

1. A multilayered flexible interconnect circuit comprising:

a first outer insulator layer;

a second outer insulator layer;

an inner insulator layer;

a first conductive layer; and

a second conductive layer, wherein:

the first outer insulator layer, the second outer insulator layer, the inner insulator layer, the first conductive layer, and the second conductive layer collectively define a busbar portion, a busbar support portion, an insulated conductor portion, and a metal-free portion of the flexible interconnect circuit,

in the busbar portion, the first conductive layer and the second conductive layer directly interface with each other while a surface of the first conductive layer facing away from the second conductive layer is exposed,

in the busbar support portion, the inner insulator layer is stacked between and directly interfaces each of the first conductive layer and the second conductive layer,

in the busbar support portion, the first conductive layer is stacked between and directly interfaces the first outer insulator layer and the inner insulator layer, and

in the busbar support portion, the second conductive layer is stacked between and directly interfaces the inner insulator layer and the second outer insulator layer.

2. The multilayered flexible interconnect circuit of claim 1, wherein, in the metal-free portion, the inner insulator layer is stacked between and directly interfaces the first outer insulator layer and the second outer insulator layer.

3. The multilayered flexible interconnect circuit of claim 2, wherein, in the insulated conductor portion:

the second conductive layer is stacked between and directly interfaces the inner insulator layer and the second outer insulator layer, and

the inner insulator layer is stacked between and directly interfaces the second conductive layer and the first outer insulator layer.

4. The multilayered flexible interconnect circuit of claim 3, wherein the insulated conductor portion is positioned between the busbar support portion and metal-free portion.

5. The multilayered flexible interconnect circuit of claim 1, wherein the busbar support portion at least partially surrounds the busbar portion.

6. The multilayered flexible interconnect circuit of claim 1, wherein the busbar support portion is positioned between the busbar portion and the metal-free portion.

7. The multilayered flexible interconnect circuit of claim 1, wherein each of the first outer insulator layer, the second outer insulator layer, the inner insulator layer, the first conductive layer, and the second conductive layer is formed from a same starting sheet.

8. The multilayered flexible interconnect circuit of claim 1, wherein each of the first outer insulator layer, the second outer insulator layer, the inner insulator layer, the first conductive layer, and the second conductive layer has the same thickness and composition throughout an entire footprint of the flexible interconnect circuit.

9. The multilayered flexible interconnect circuit of claim 1, wherein each of the first outer insulator layer, the second outer insulator layer, and the inner insulator layer has an opening in the busbar portion.

10. The multilayered flexible interconnect circuit of claim 1, wherein:

each of the first outer insulator layer and the second outer insulator layer comprises a polymer base and an adhesive layer covering a surface of and supported by the polymer base,

the polymer base comprises one or more polymers selected from the group consisting of polyimide (PI), polyethylene naphthalate (PEN), polyethylene terephthalate (PET), polymethyl methacrylate (PMMA), ethyl vinyl acetate (EVA), polyethylene (PE), polyvinyl fluoride (PVF), polyamide (PA), and/or polyvinyl butyral (PVB), and

the adhesive layer comprises one or more of epoxy and polyurethane.

11. The multilayered flexible interconnect circuit of claim 10, wherein, in the busbar support portion:

the adhesive layer of the first outer insulator layer directly interfaces and is adhered to the first conductive layer, and

the adhesive layer of the second outer insulator layer directly interfaces and is adhered to the second conductive layer.

12. The multilayered flexible interconnect circuit of claim 1, wherein:

the inner insulator layer comprises an inner polymer base, a first inner adhesive layer, and a second inner adhesive layer,

the inner polymer base is positioned between and supports each of the first inner adhesive layer and the second inner adhesive layer,

the inner polymer base comprises one or more polymers selected from the group consisting of polyimide (PI), polyethylene naphthalate (PEN), polyethylene terephthalate (PET), polymethyl methacrylate (PMMA), ethyl vinyl acetate (EVA), polyethylene (PE), polyvinyl fluoride (PVF), polyamide (PA), and/or polyvinyl butyral (PVB), and

each of the first inner adhesive layer and the second inner adhesive layer comprises one or more of epoxy and polyurethane.

13. The multilayered flexible interconnect circuit of claim 12, wherein, in the busbar support portion:

the first inner adhesive layer of the inner insulator layer directly interfaces and is adhered to the first conductive layer, and

the adhesive layer of the second outer insulator layer directly interfaces and is adhered to the second conductive layer.

14. The multilayered flexible interconnect circuit of claim 1, wherein each of the first conductive layer and the second conductive layer comprises aluminum and has a thickness of 100-400 micrometers.

15. The multilayered flexible interconnect circuit of claim 1, further comprising a support unit adhered to the first outer insulator layer and comprises a busbar access opening such that the busbar portion fully overlaps with the support unit.

16. The multilayered flexible interconnect circuit of claim 1, wherein the first outer insulator layer and second outer insulator layer comprise a set of flexibility slits in the metal-free portion surrounding the busbar support portion thereby providing out-of-plane flexibility of the busbar portion.

17. The multilayered flexible interconnect circuit of claim 1, further comprising a registration portion comprising:

a first registration opening in the second outer insulator layer; and

a second registration opening in the second conductive layer, wherein:

a dimension of the first registration opening in a direction is larger than a dimension of the second registration opening in the same direction,

the first registration opening and the second registration opening are aligned,

a portion of the second conductive layer is visible through the first registration opening, and

a portion of an insulator layer other than the second outer insulator layer is visible through the second registration opening.

18. The multilayered flexible interconnect circuit of claim 17, wherein the portion of an insulator layer other than the second outer insulator layer visible through the second registration opening is a portion of the inner insulator layer.

19. The multilayered flexible interconnect circuit of claim 1, further comprising at least one high-current conductor electrically unconnected with any of the busbars and comprising at least two conductive layers that directly interface one another.

20. The multilayered flexible interconnect circuit of claim 19, wherein the high-current conductor comprises at least one heatsink portion and at least one intersink portion, wherein:

the heatsink portion and intersink portion are monolithic,

the heatsink portion extends further in a width than the intersink portion, and

a ratio of an extension of the heatsink portion in the width to an extension of the intersink portion in the same direction is at least 10:1.

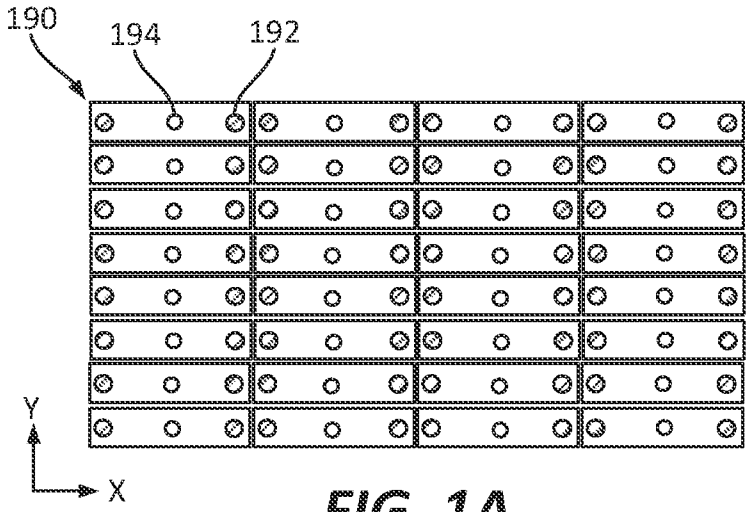

FIG. 1A

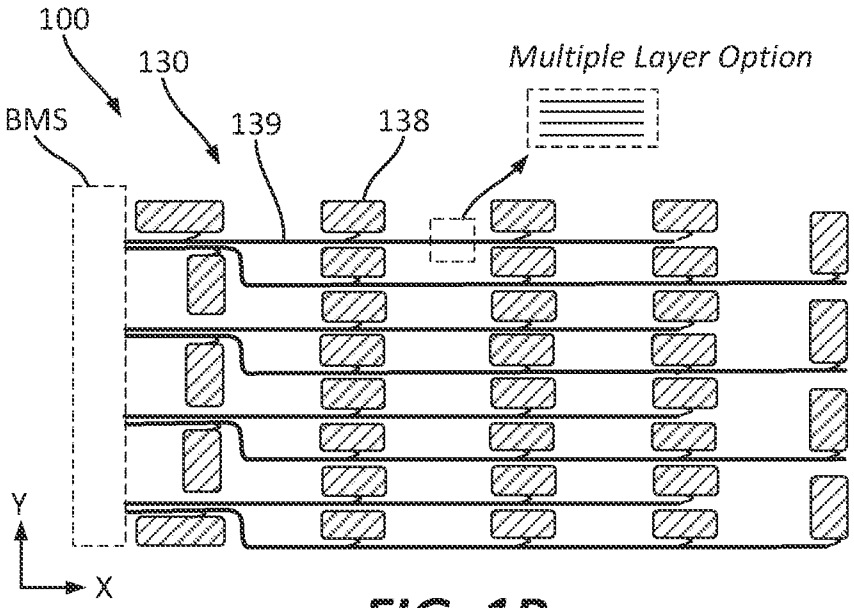

FIG. 1B

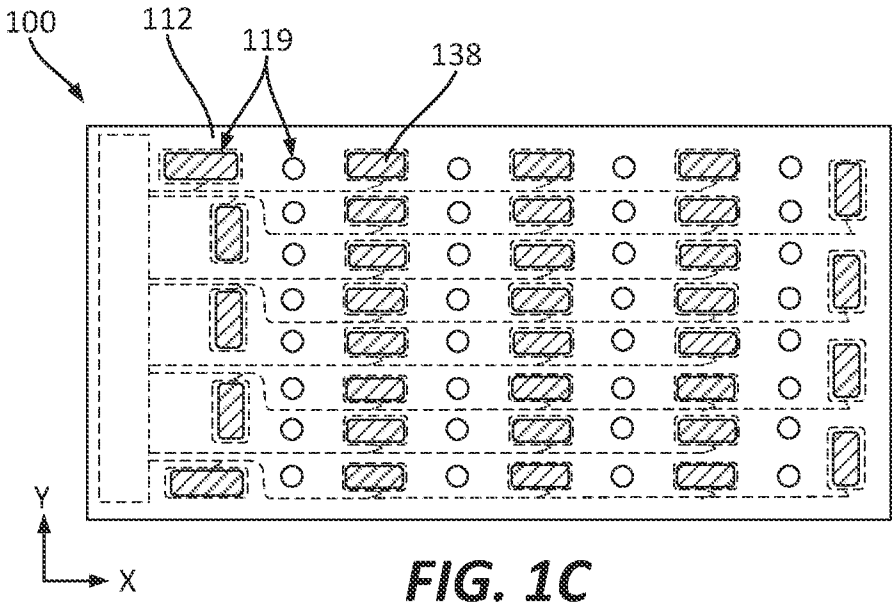

FIG. 1C

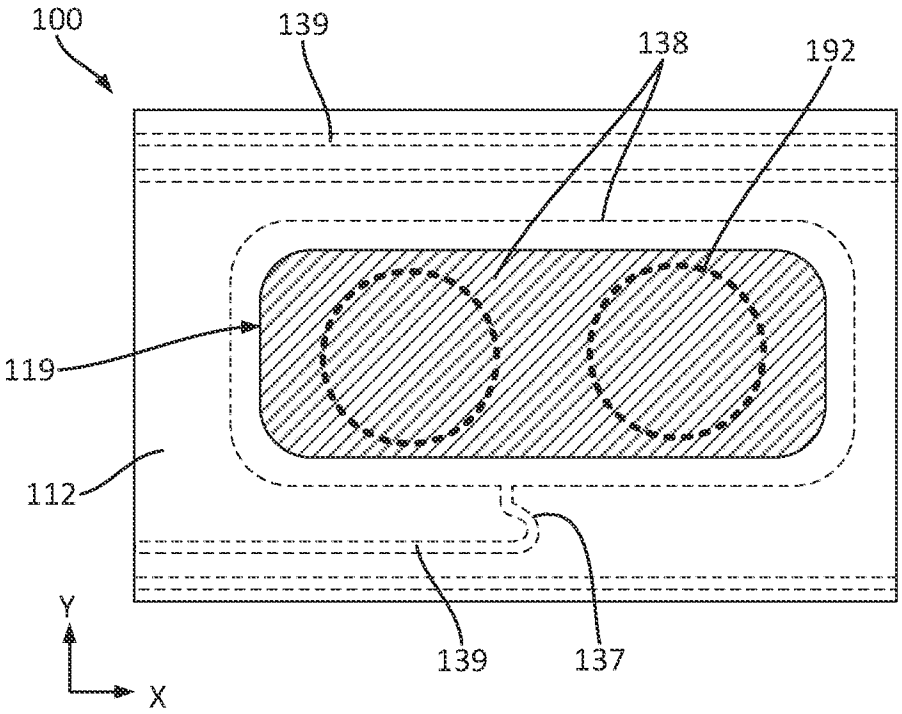
100
139
138
192
119
112
139
137
Y
X

FIG. 1D

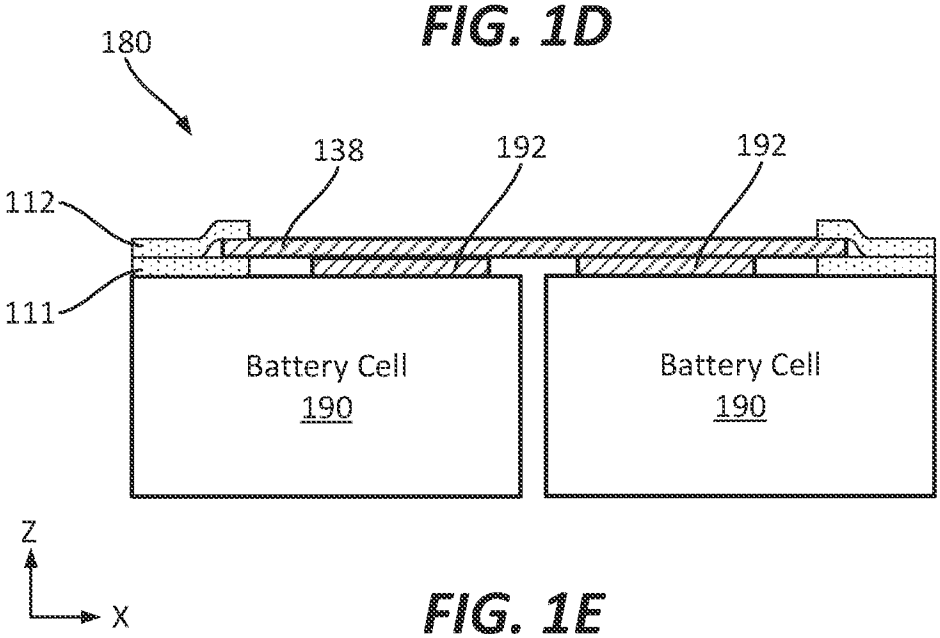
180
138
192
192
112
111
Battery Cell
190
Battery Cell
190
Z
X

FIG. 1E

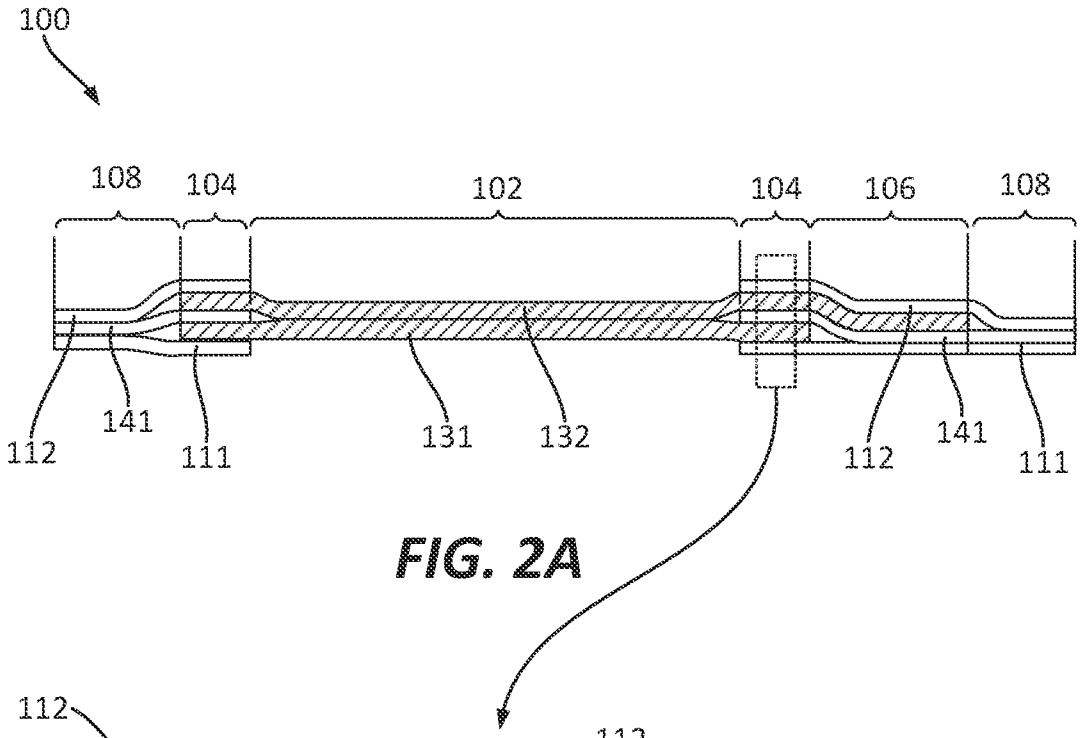

FIG. 2A

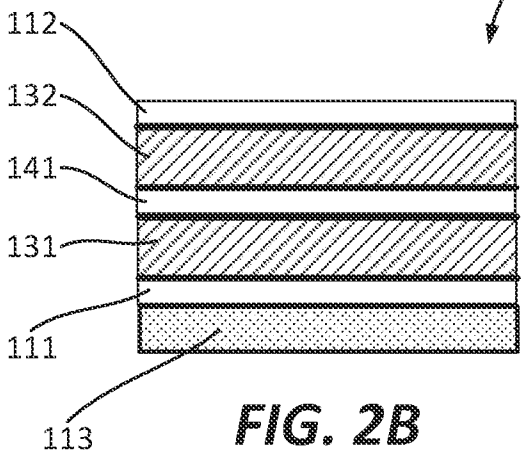

FIG. 2B

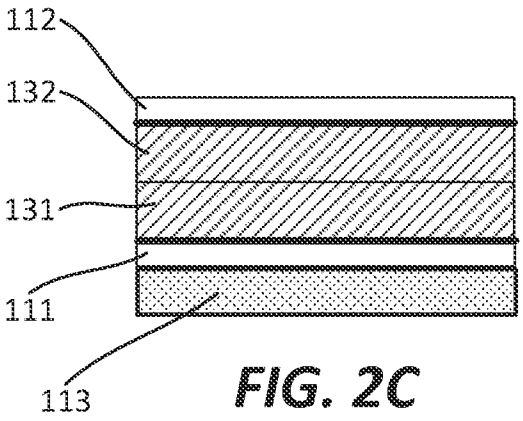

FIG. 2C

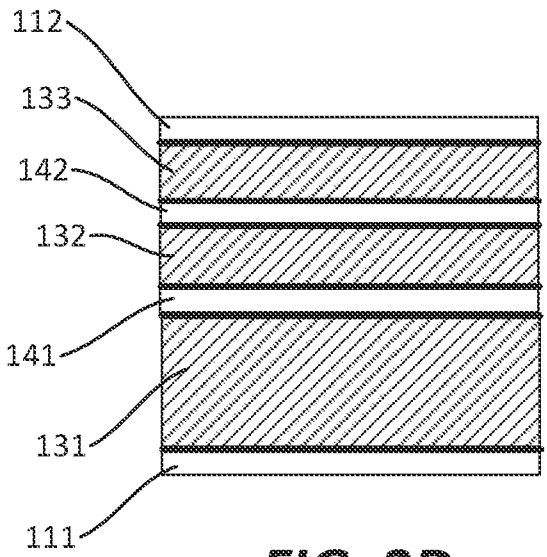

FIG. 2D

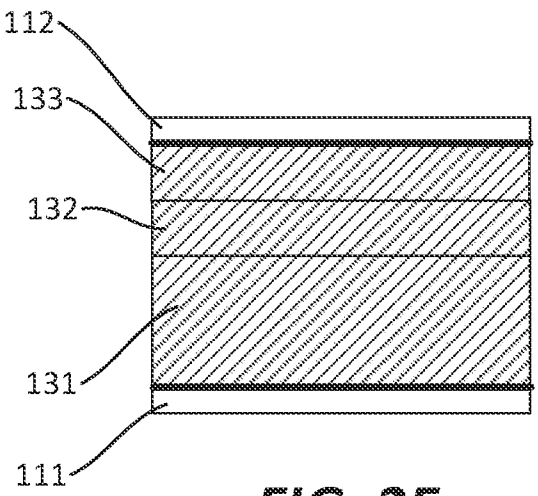

FIG. 2E

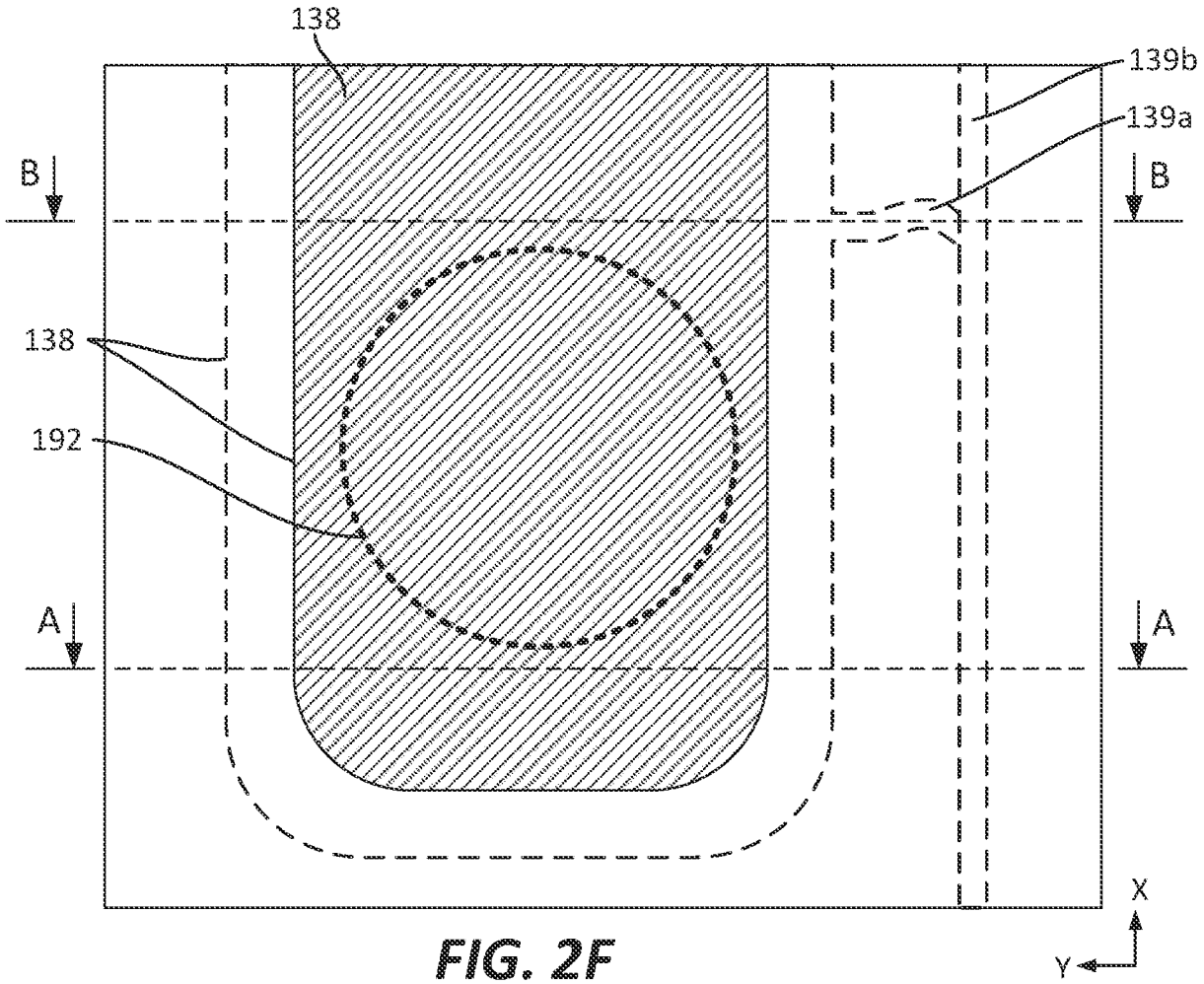

FIG. 2F

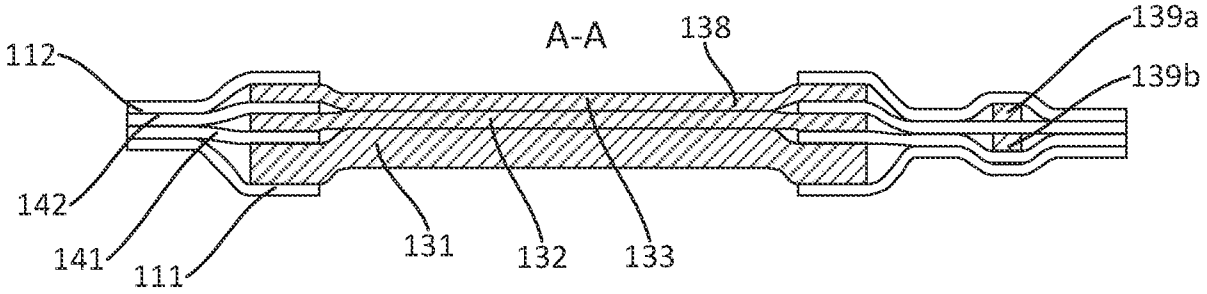

FIG. 2G

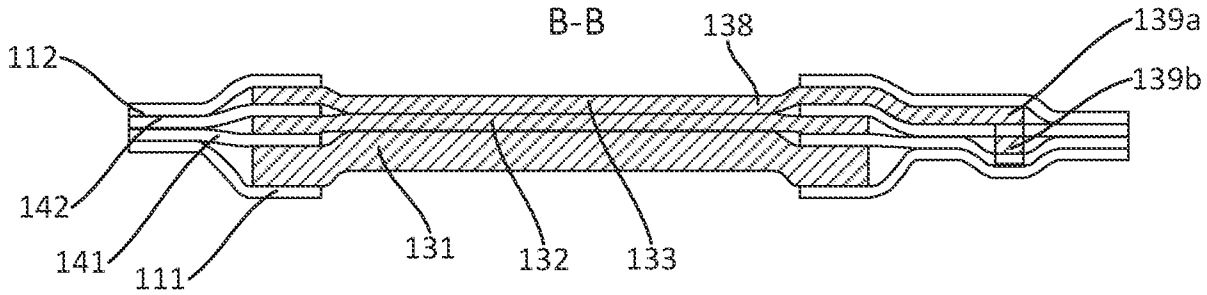

FIG. 2H

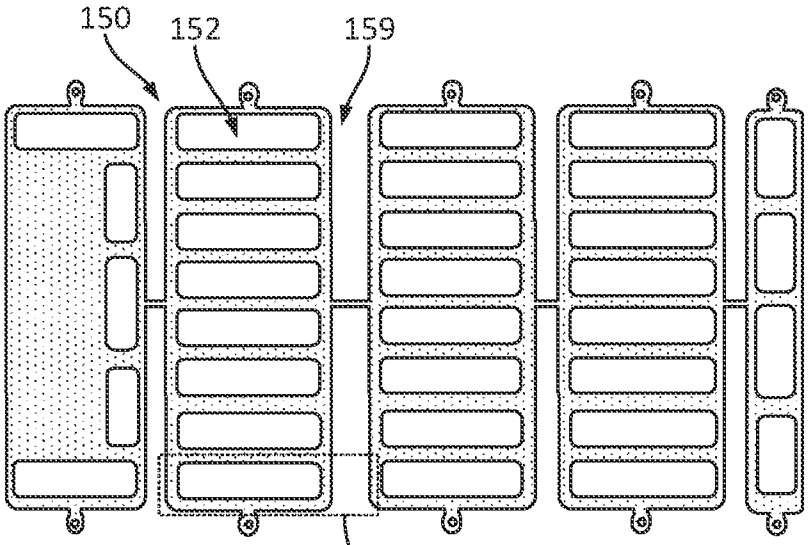

FIG. 3A

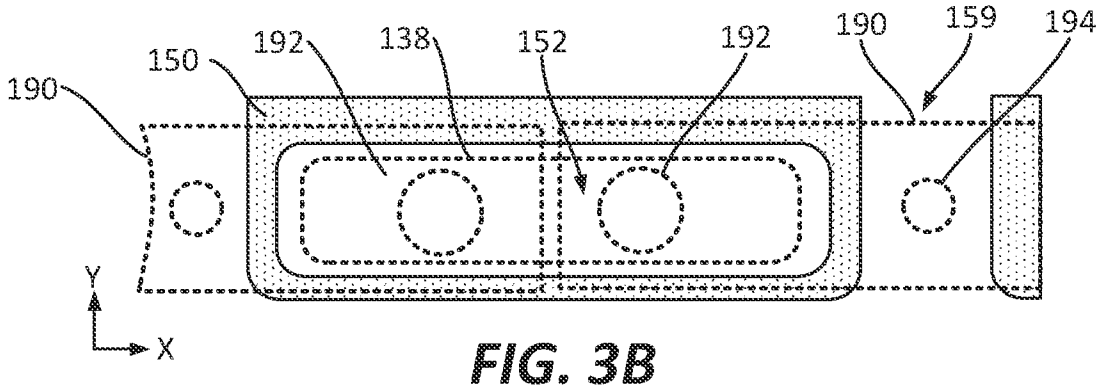

FIG. 3B

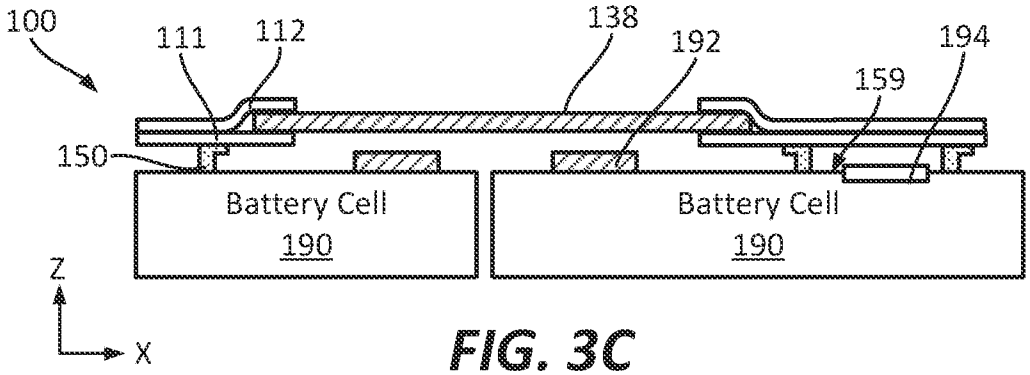

FIG. 3C

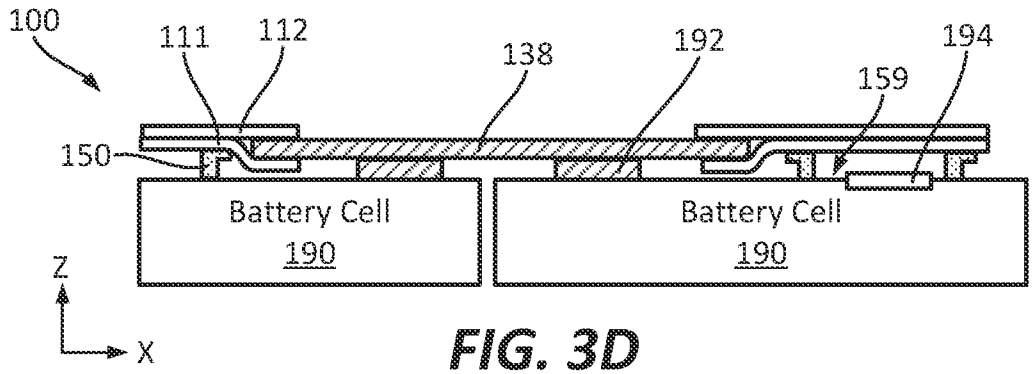

FIG. 3D

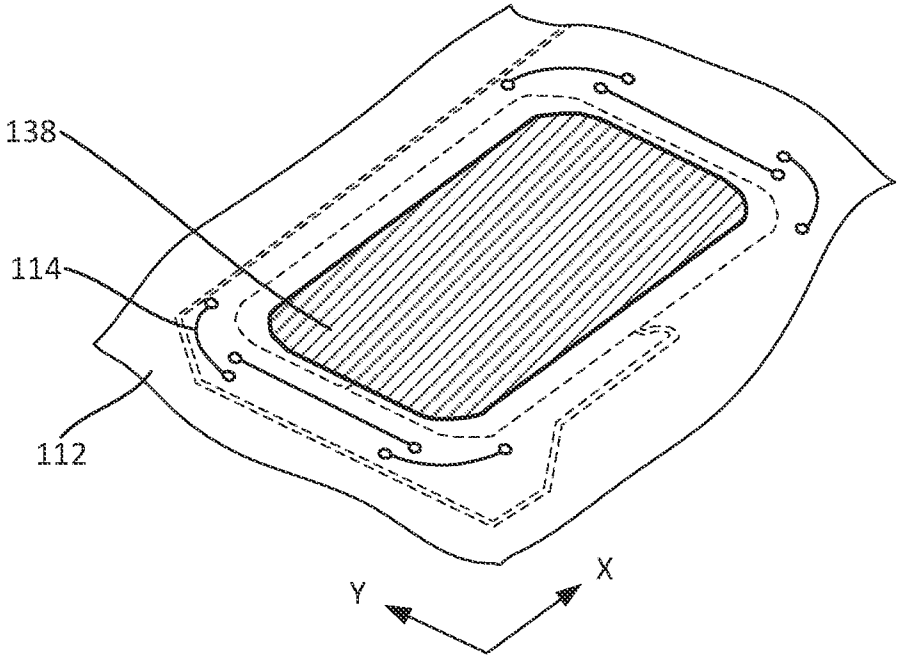

FIG. 3E

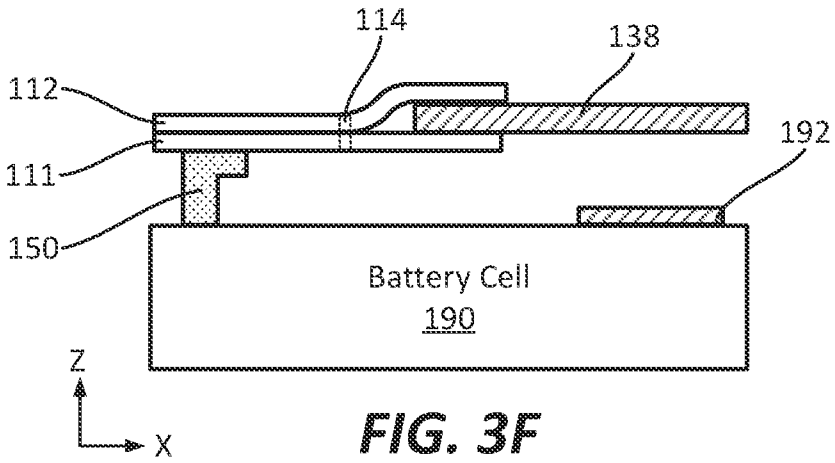

FIG. 3F

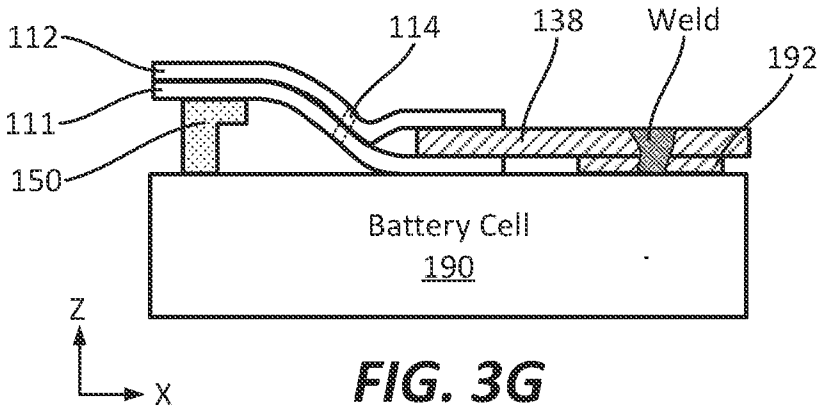

FIG. 3G

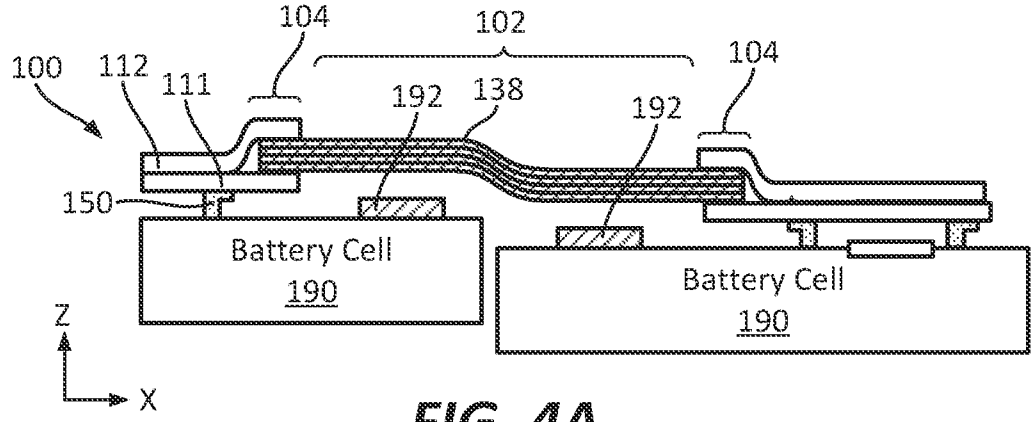
104
102
104
100
112
111
192
138
192
150
Battery Cell
190
Battery Cell
190
Z
X

FIG. 4A

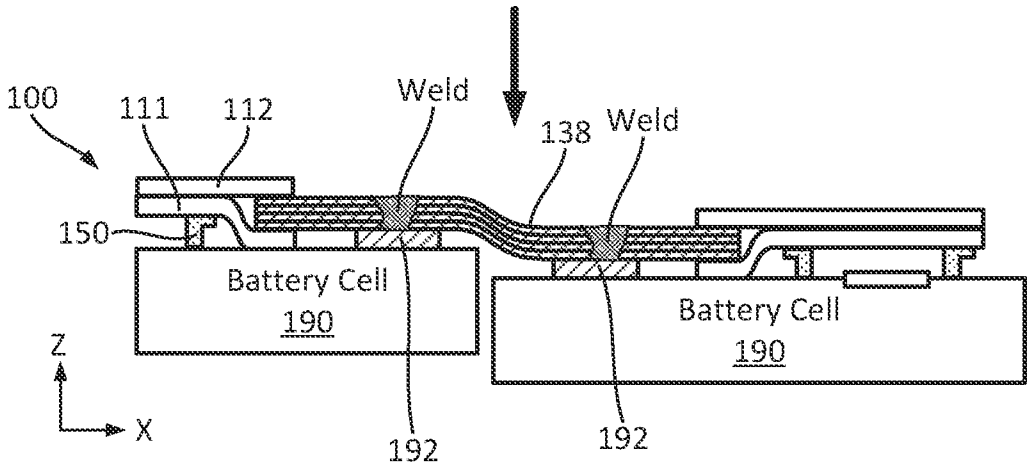
100
111
112
Weld
138
Weld
150
Battery Cell
190
Battery Cell
190
Z
X
192
192

FIG. 4B

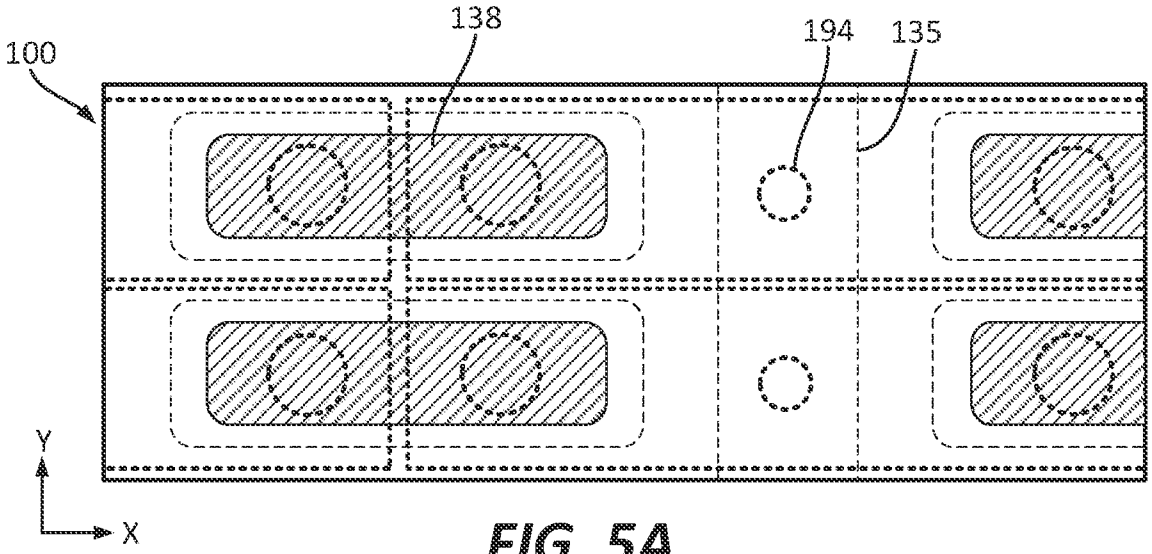

FIG. 5A

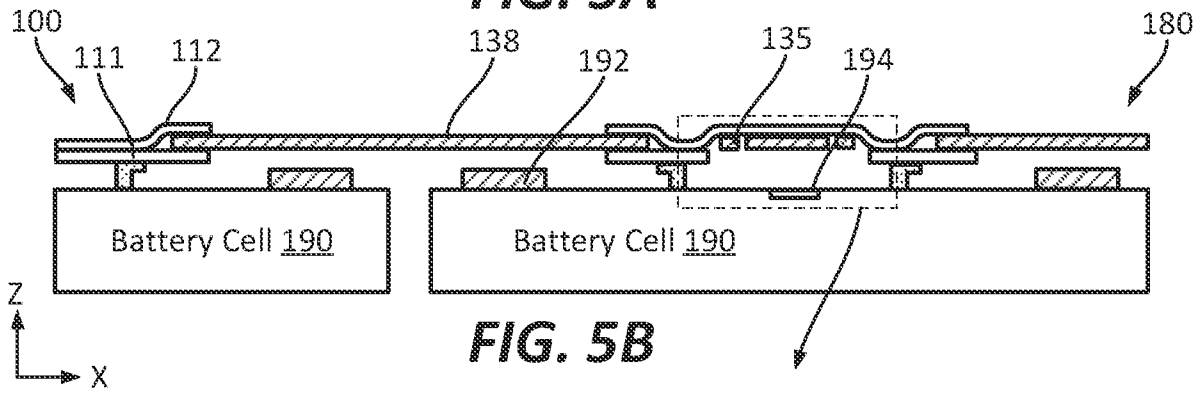

FIG. 5B

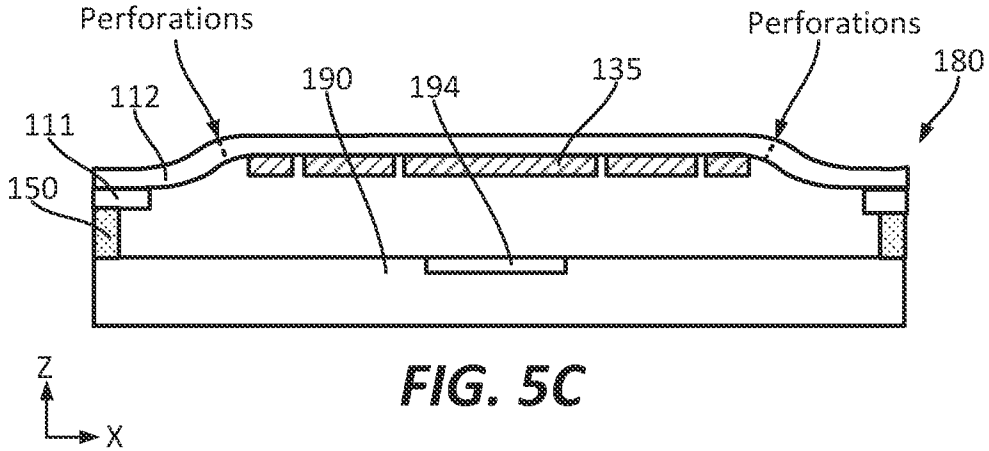

FIG. 5C

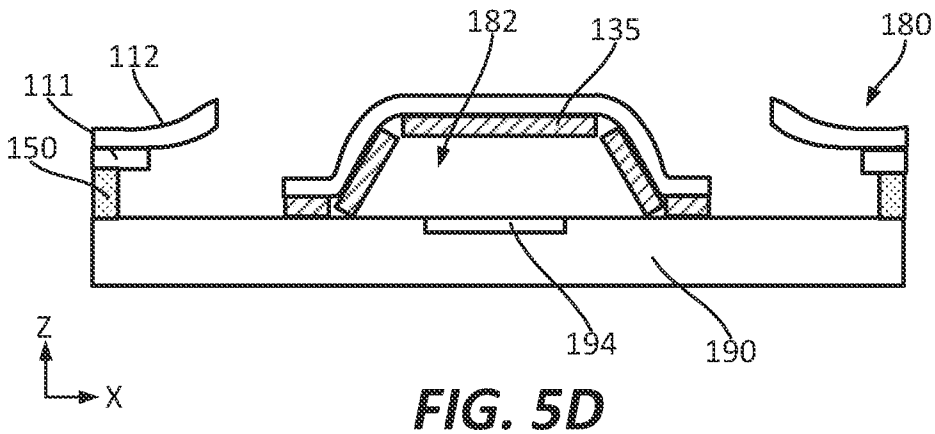

FIG. 5D

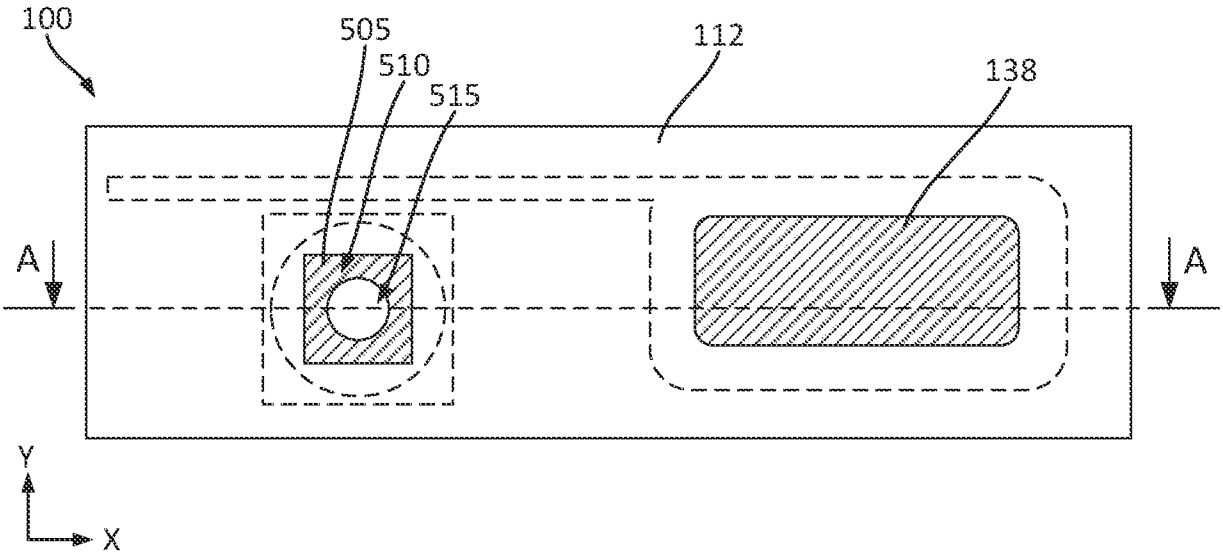

FIG. 5E

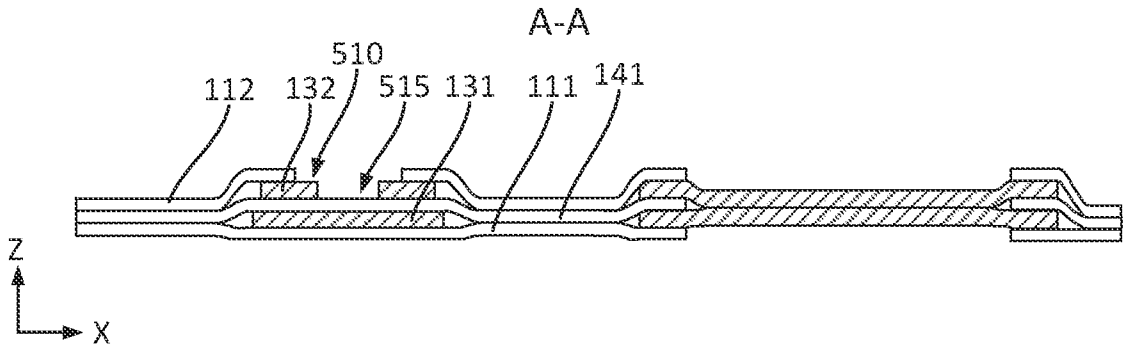

FIG. 5F

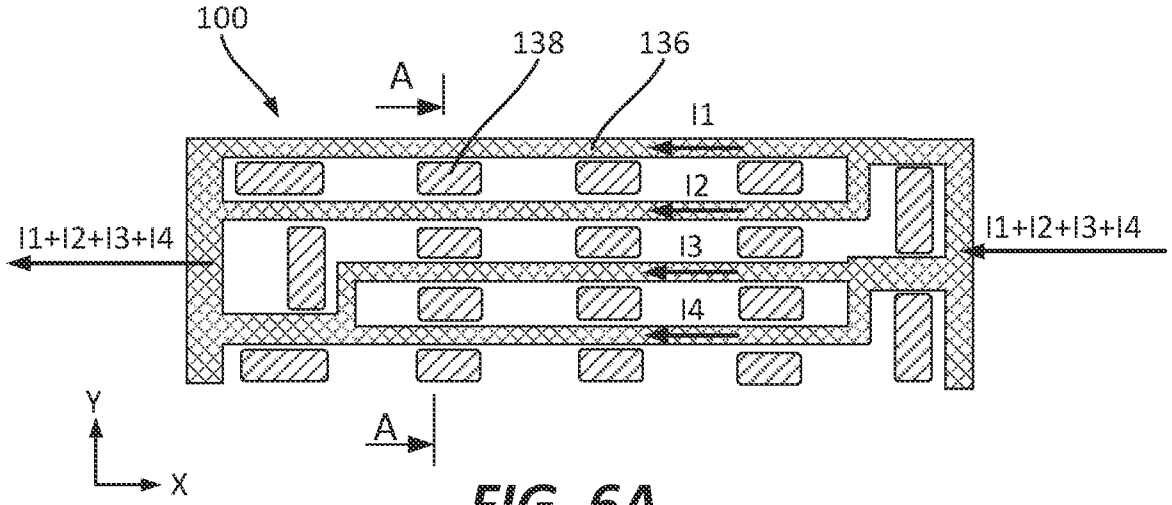

FIG. 6A

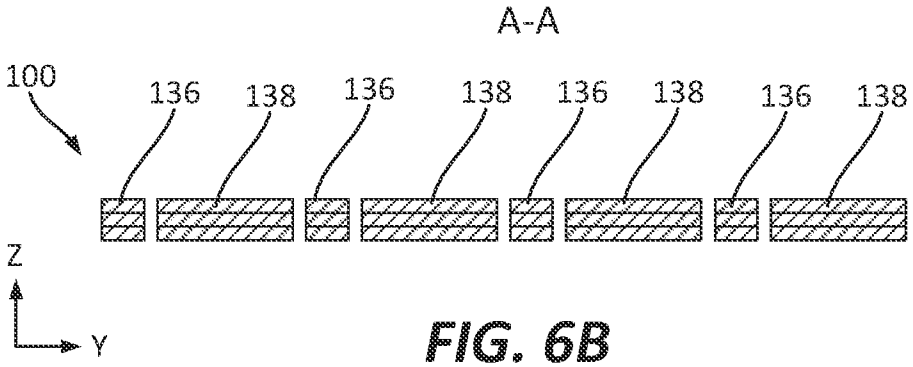

FIG. 6B

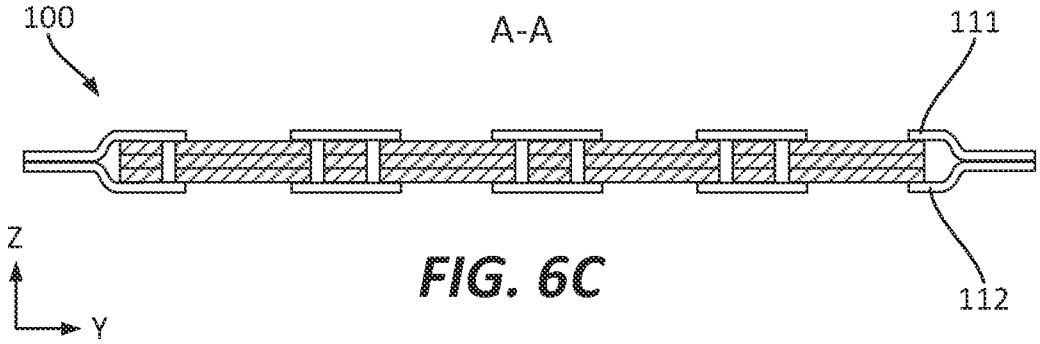

FIG. 6C

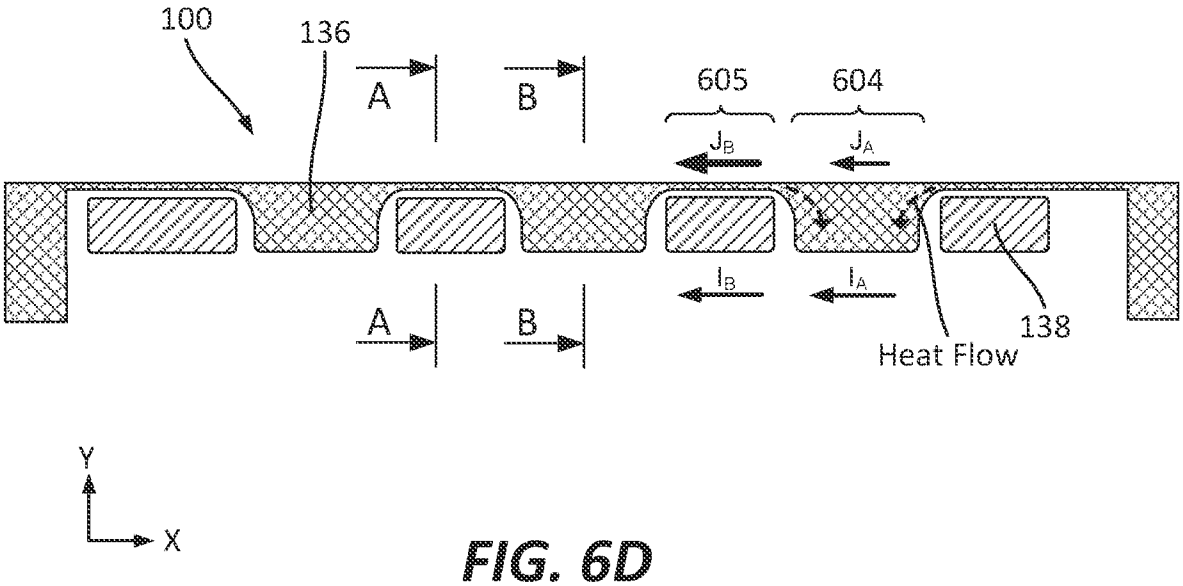

FIG. 6D

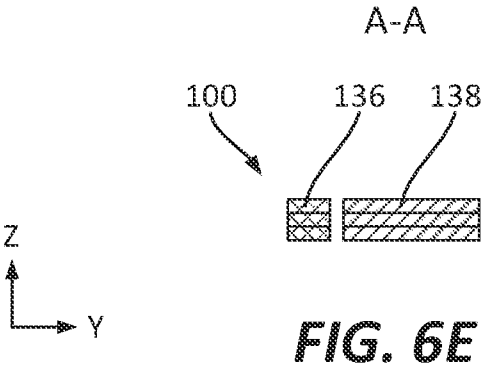

FIG. 6E

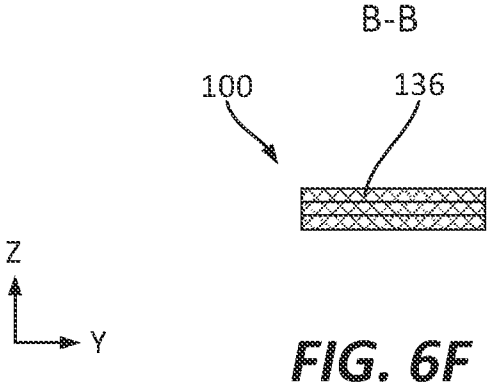

FIG. 6F

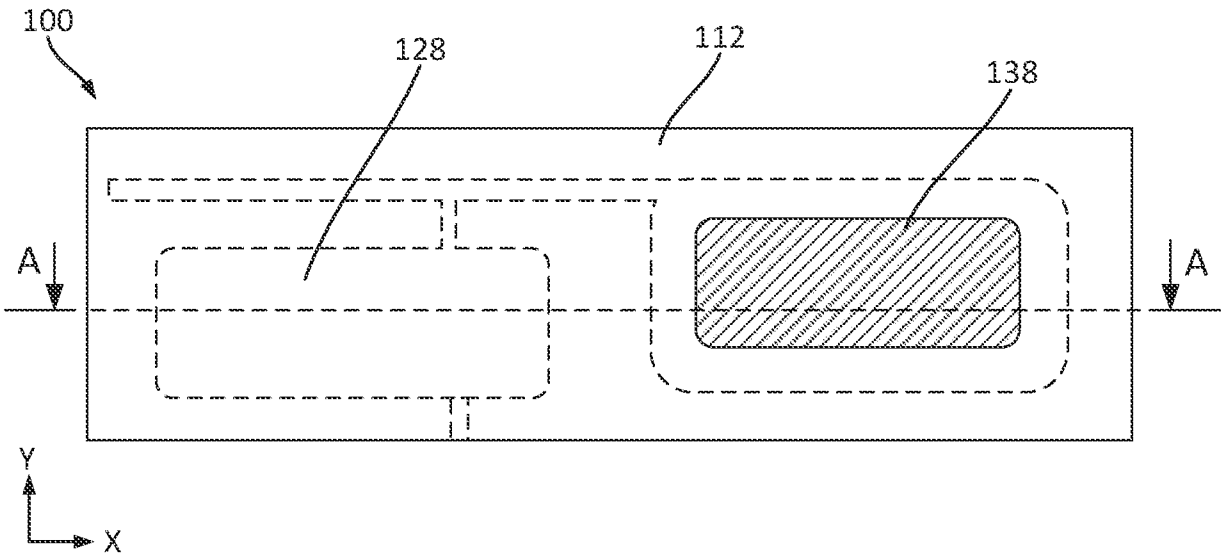

FIG. 7A

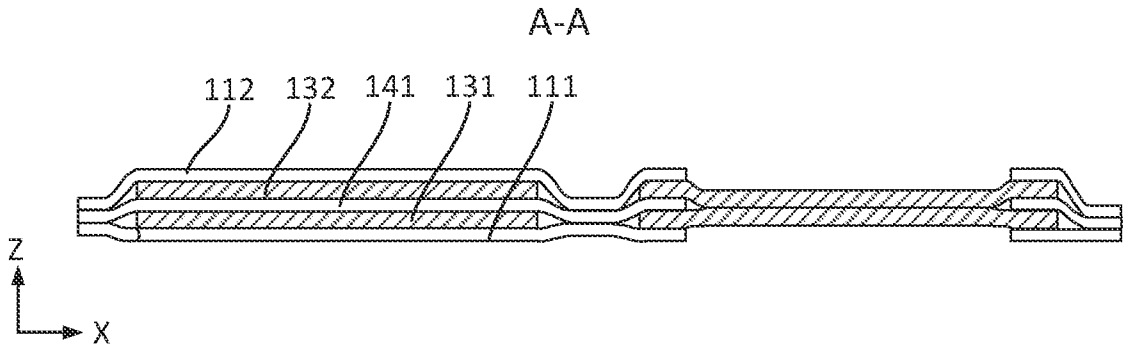

FIG. 7B

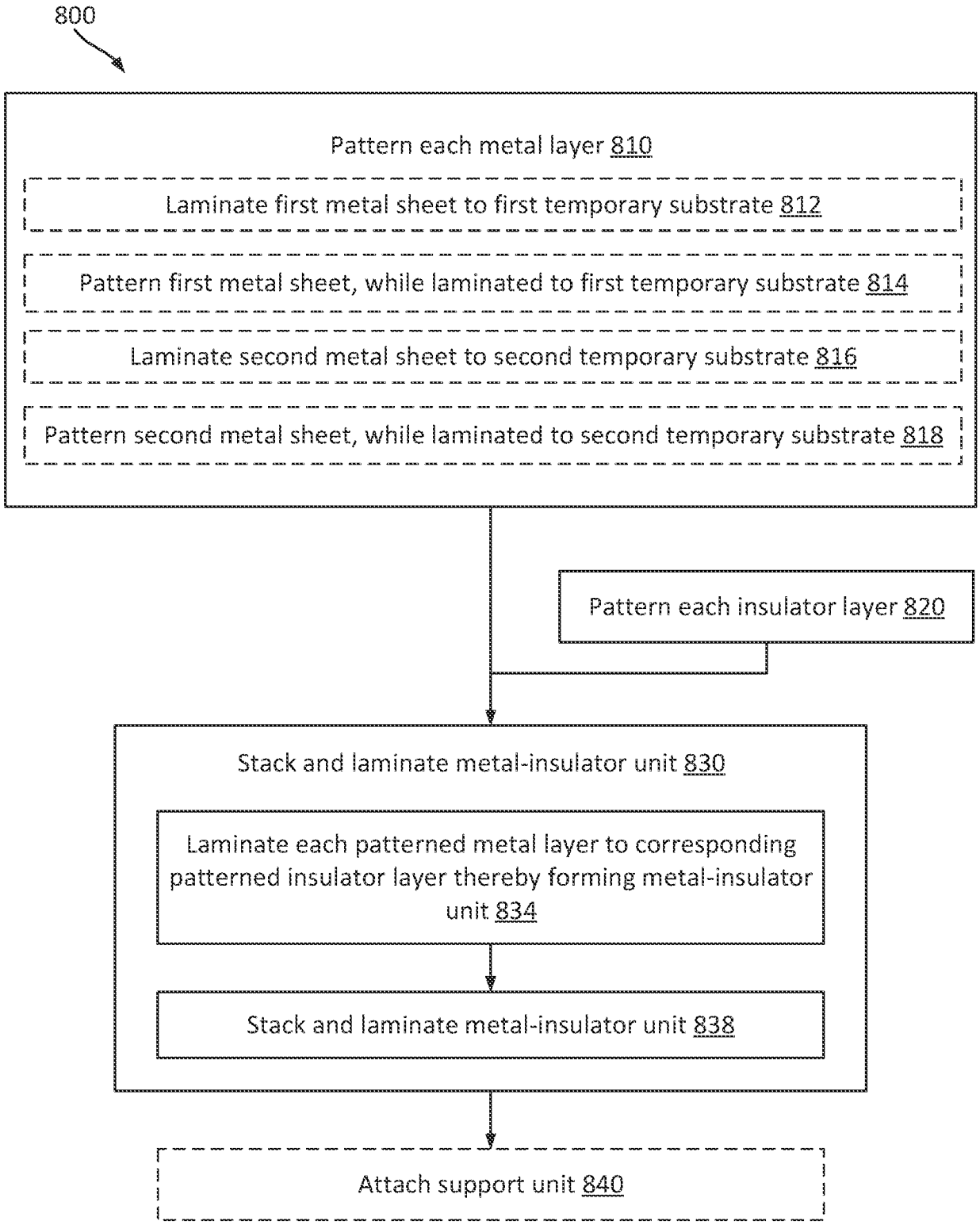
800
Pattern each metal layer 810
Laminate first metal sheet to first temporary substrate 812
Pattern first metal sheet, while laminated to first temporary substrate 814
Laminate second metal sheet to second temporary substrate 816
Pattern second metal sheet, while laminated to second temporary substrate 818
Pattern each insulator layer 820
Stack and laminate metal-insulator unit 830
Laminate each patterned metal layer to corresponding patterned insulator layer thereby forming metal-insulator unit 834
Stack and laminate metal-insulator unit 838
Attach support unit 840

FIG. 8

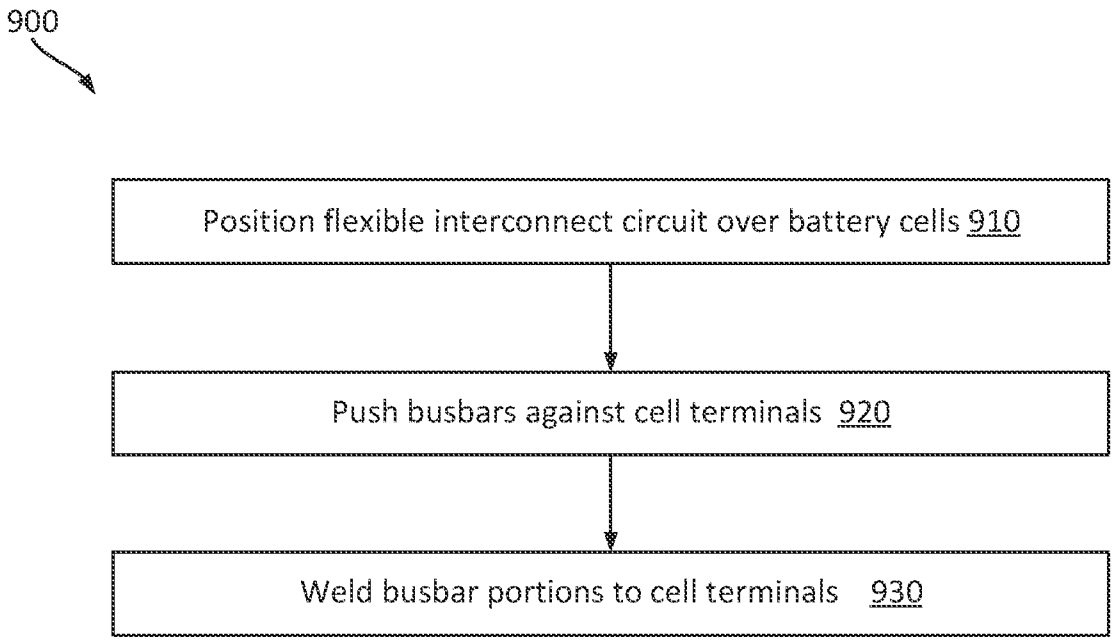
900
Position flexible interconnect circuit over battery cells 910
Push busbars against cell terminals 920
Weld busbar portions to cell terminals 930

FIG. 9

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2024/052532

A. CLASSIFICATION OF SUBJECT MATTER

H01M 50/526(2021.01)i; **H01M 50/524**(2021.01)i; **H01M 50/503**(2021.01)i; **H01M 50/505**(2021.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01M 50/526(2021.01); H01B 11/06(2006.01); H01B 7/00(2006.01); H01B 7/02(2006.01); H01B 7/08(2006.01); H01M 10/48(2006.01); H01M 2/10(2006.01); H01M 2/20(2006.01); H01M 50/20(2021.01); H05K 1/14(2006.01)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: busbar, interconnect, flexible, insulator, circuit

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 2023-201030 A2 (CELLINK CORPORATION) 19 October 2023 (2023-10-19) claims 1, 21; paragraph [00100]; figure 6A	1-20
A	KR 10-2021-0038826 A (SAMSUNG SDI CO., LTD.) 08 April 2021 (2021-04-08) abstract; claim 1	1-20
A	KR 10-2007-0043496 A (LG CHEM, LTD.) 25 April 2007 (2007-04-25) abstract; claim 1	1-20
A	CN 208045121 U (ZHEJIANG PU METAL MANUFACTURING CO., LTD.) 02 November 2018 (2018-11-02) abstract; claims 1, 2	1-20
A	CN 102044310 A (YIDING CO., LTD.) 04 May 2011 (2011-05-04) abstract; claim 1; figure 1	1-20

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"D" document cited by the applicant in the international application
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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
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"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 February 2025	**13 February 2025**

Name and mailing address of the ISA/KR	Authorized officer
Korean Intellectual Property Office **189 Cheongsa-ro, Seo-gu, Daejeon** **35208, Republic of Korea**	**LEE, Kang Ha**
Facsimile No. **+82-42-481-8578**	Telephone No. **+82-42-481-5687**

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/US2024/052532

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		US 2024-0215173 A1	27 June 2024
		WO 2023-201030 A3	23 November 2023
KR 10-2021-0038826 A	08 April 2021	EP 3799148 A1	31 March 2021
		EP 3799148 B1	15 November 2023
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KR 10-2007-0043496 A	25 April 2007	KR 10-0946579 B1	09 March 2010
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CN 102044310 A	04 May 2011	CN 102044310 B	07 May 2014
		HK 1153847 A1	05 April 2012