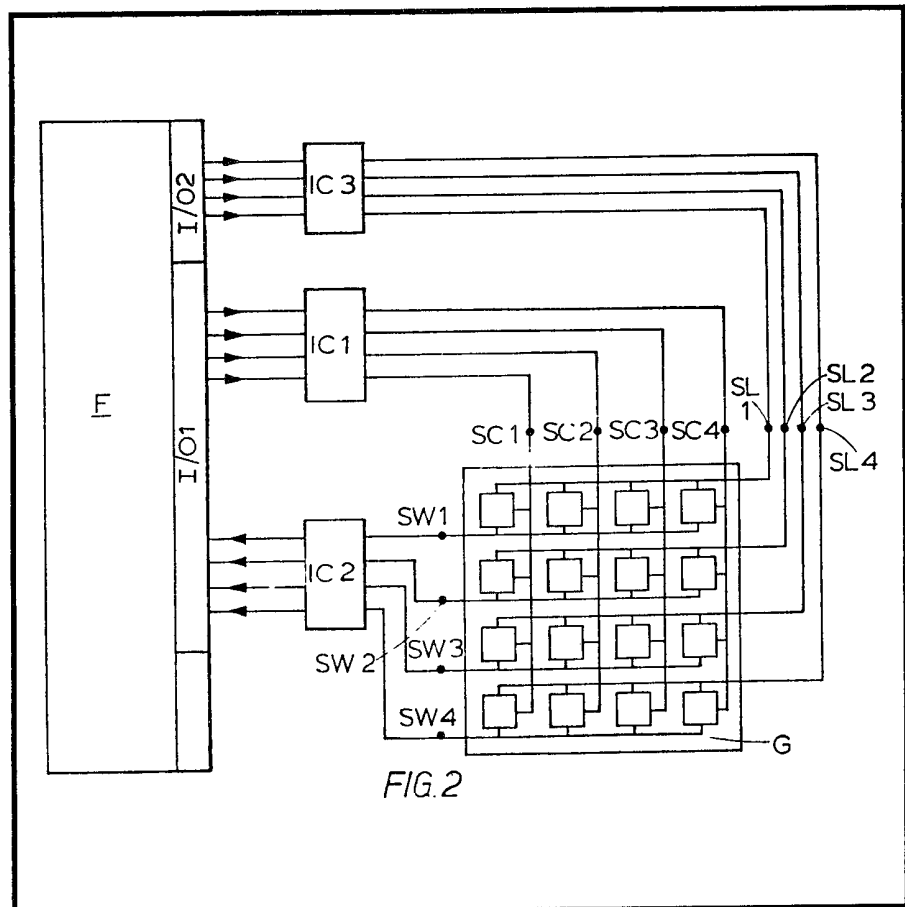


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**(54) Supervision of touch control switches**

(57) A matrix array of touch control switches is supervised by a micro-processor (F) to ascertain which of the switches is in an operated state. Inputs (SC1 . . . 4) are each connected to all the switches in a respective column and outputs (SW1 . . . 4) are connected to all the switches of a row or group. Pulsed 'read' signals fed repeatedly to the inputs in turn are compared with the resulting signals at the outputs, and a switch in an operated state produces a reduced output, which a circuit (IC2) does not pass on. The switches can be of the kind incorporating an illuminating phosphor (P), as forming the subject of the parent application 31638/78, and illumination control signals fed from the microprocessor (F) and applied to

the electrode (E) on the phosphor are used in conjunction with signals fed to the 'read' inputs (SC1 . . . 4) to illuminate selected switches.



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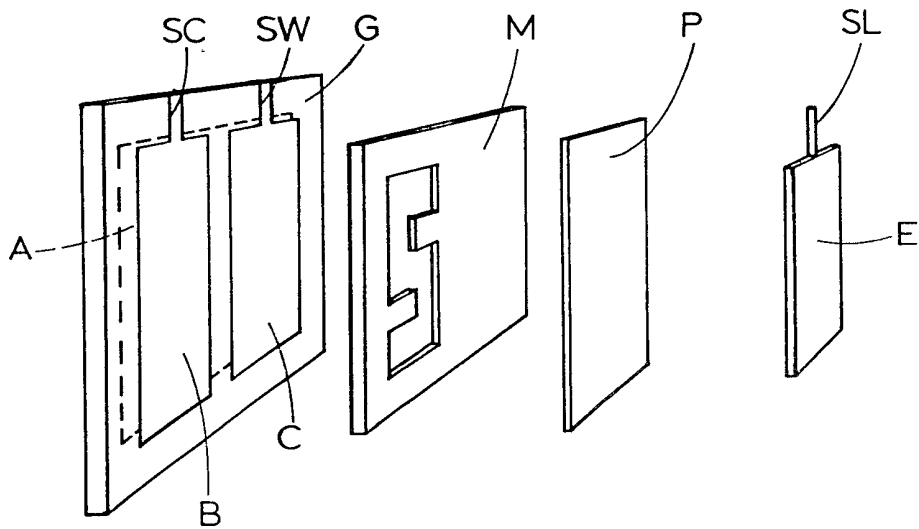


FIG. 1

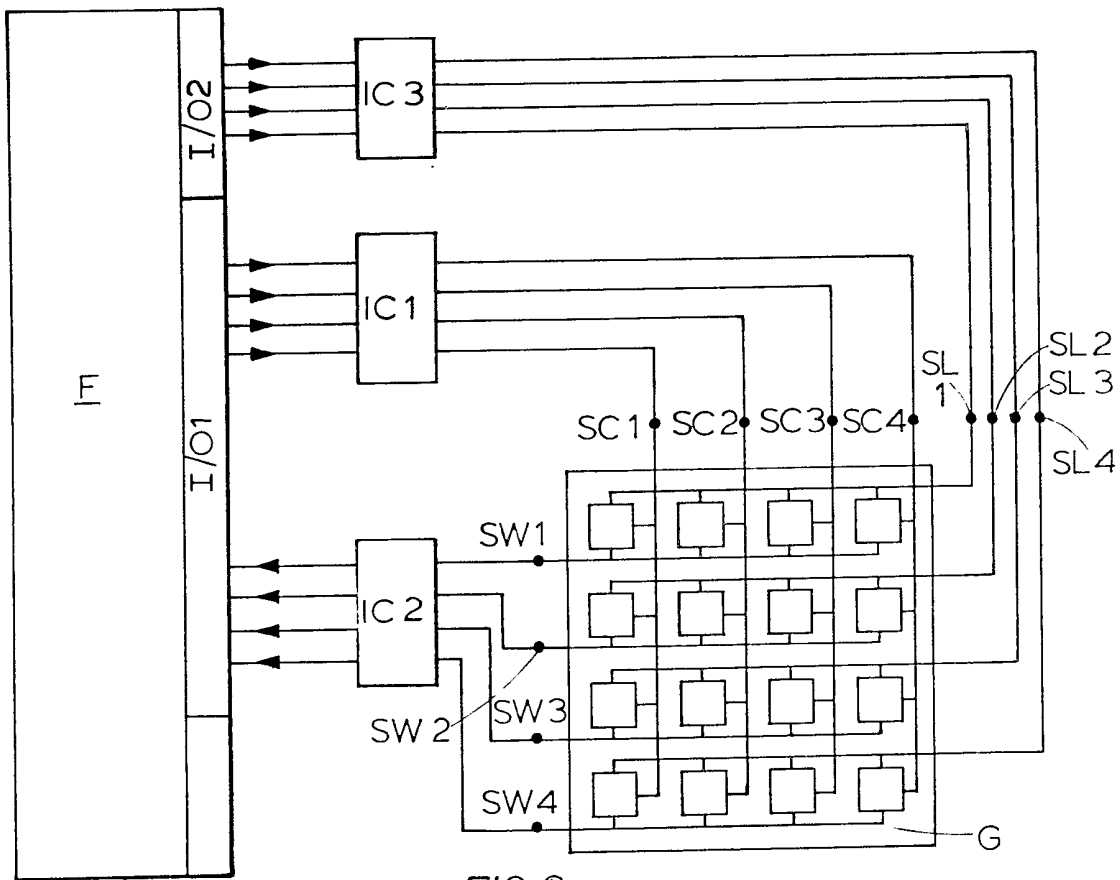


FIG. 2

## SPECIFICATION

**Supervision of touch control switches**

5 This invention relates to means employing a processor, in particular a microprocessor, for supervising an array of touch control switches to determine the state of each switch, i.e. whether it is operated or not operated. It is applicable to touch control switches in general, but is of particular application where the switches are of a kind incorporating a luminescent display, such as form the subject of our co-pending patent application No. 31638/78 (Serial No. 2002522) from which the present application has been divided.

According to the invention there is proposed a matrix array of touch control switches arranged in  $n$  groups of  $m$  switches in each group, with  $m$  'read' inputs, each of which is connected to a respective set of said switches comprising one from each group, and  $n$  'read' outputs, each of which is connected to all of the switches of a respective group; and a processor connected to the said 'read' inputs and outputs and acting so as to apply a 'read' signal to each of the inputs in succession and to analyse the resultant signals appearing at the outputs on each application of the 'read' signal and thereby to determine whether any of the respective set of switches is in an operated state.

Preferably the 'read' signal is applied to each 'read' input a predetermined plurality of times during each 'read' cycle so that the processor reads the state of each set of switches that plurality of times and only responds if the same pattern of signals corresponding to a control function occurs at the 'read' outputs each time.

The 'read' signal applied to the inputs may be a pulse signal so that there appears at the 'read' output of a switch that is in an operated state an output pulse signal of reduced amplitude, each 'read' output being connected to the processor via a circuit that passes the output pulse signal to the processor only if that signal is above a predetermined threshold corresponding to the lower limit of the amplitude of 'read' output pulse signals from a switch that is in a non-operated state.

The switches themselves may be of the form defined in Claim 1 of the parent application, in which case there may in addition be illumination control inputs, each of which is connected to the electrodes of all the switches of a respective group, the processor being connected to the 'read' control inputs and illumination control inputs so as to apply signals thereto to illuminate selected switches.

The invention will now be described by way of example with reference to the accompanying drawings, in which:—

*Figure 1* is an exploded schematic diagram of a touch control switch of the kind used in

the preferred embodiment of the invention;

*Figure 2* is a schematic diagram showing a matrix array of the switches of Fig. 1 and all under the supervision of a microprocessor in the manner according to the invention.

The touch control switch illustrated in Fig. 1 forms the subject of our co-pending patent application No. 31638/78 (Serial No. 2 002 522) from which the present application was divided, and for a detailed description of it reference should be made to that application. The switch comprises dielectric a panel G of glass with a single conductive layer A applied to its front face and two similar conductive layers B, C applied to its rear face alongside one another in super-imposed relationship with the layer A. An input connection SC is provided for the layer B and an output connection SW for the layer C, so that 'read' pulses can be fed into the layer B to induce output pulses in the layer C by virtue of the capacitive coupling between the two layers B, C via the layer A. If the layer A is touched, the capacitive characteristics of the switch change, causing the amplitude of the output pulses from the layer C to fall and to trigger a control function in the external supervisory circuit described below.

The switch also has an electro-luminescent phosphor layer P behind the layer B and an electrode E on the back of the phosphor layer, with a connection SL for feeding illumination control signals to the electrode E. The layer P will be illuminated by the presence of a predetermined minimum potential between the electrode E and the layer B. The layer A and B are transparent so that the illumination is visible from the front of the switch and, as shown, there can be an opaque mask M interposed between the panel G and the phosphor layer P so that a symbol (in this case the numeral '2') is formed.

If a positive potential is applied to the layer B of insufficient magnitude to excite the phosphor when the electrode E is at earth potential, but sufficient to excite it when an appropriate negative potential is present at the electrode E, then the application of the positive potential to the layer B can serve not only to sense the state of the switch but also to excite the phosphor under the control of the illumination control signal.

Turning now to Fig. 2, this illustrates a  $4 \times 4$  multiplexed array of switches, each of the kind illustrated in Fig. 1, with the 'read' input connections SC, illumination control input connections SL and output connections SW, all connected to supervisory circuitry comprising a microprocessor F. The switches are shown arranged in rows and columns with the 'read' input connections SC of the four switches in each column connected to a common input terminal SC1, SC2, SC3 or SC4, and with the output connections SW of the four switches in each row connected to a

common output terminal SW1, SW2, SW3 or SW4.

The microprocessor F has an 8-bit input/output port I/O1 with four output connections connected via a voltage amplifier IC1 to the four 'read' input connections SC1 to SC4 of the switch array, and with four input connections connected via a buffer circuit IC2 to the output connections SW1 to SW4 of the switch array. The microprocessor produces a succession of square 'read' pulses with an amplitude of 5 volts and these are transformed into 50 volt pulses by the amplifier IC1 and applied to the 'read' input connections SC1 to SC4 of the array. The resultant output pulses from the output connections SW1 to SW4 are peaked pulses due to the capacitive nature of the contact switches but the decay rate of these pulses is limited by virtue of the buffer circuit IC2 having a high input impedance. If, at the time a pulse is applied to the input SC of a given switch, that switch is in a operated state (by virtue of the presence of a user's finger at its layer A) the amplitude of the resulting output pulse at its connection SW is reduced, and it falls below a threshold level set in the buffer circuit IC2 so that the latter does not pass the pulse to the microprocessor. If a switch is not operated, however, the output pulse from it causes the buffer circuit IC2 to pass a corresponding output pulse to the microprocessor. Further, the buffer circuit IC2 is such that the resulting output pulses that it passes to the microprocessor are substantially square pulses with an amplitude and length similar to those of the output pulses from the microprocessor. This enables the input and output pulses to be analysed together in the microprocessor to determine which if any of the switches in the array has been operated.

In an alternative embodiment, the buffer circuit IC2 could be replaced by four comparators each with a first input from a respective one of the output terminals SW1 to SW4 and a second input from a potential divider that sets a threshold potential for the comparator corresponding to a level that discriminates between output pulses from an operated and non-operated switch. An advantage of this arrangement is that, by using the same power supply for the potential divider and for the 'read' pulses, a wider variation in supply voltage can be tolerated as compared with the arrangement of the buffer circuit IC2.

In operation, the microprocessor F applies four 'read' pulses to each of the inputs SC1 to SC4 in turn. If none of the four switches in the column associated with an input connection is in a operated state, they pass output pulses via the output connections SW1 to SW4 back to the microprocessor each time they are read. However, if one of the switches has been operated, it inhibits the passage of a pulse to the output connection associated with

the row of switches in which that switch lies. Each time each column is read, the microprocessor looks for the lack of a pulse on a respective one of the output connections to see if the corresponding switch in that row of switches has been operated. The four 'read' pulses applied to each column therefore effectively read each in turn of the four switches in that column to see if it has been operated, and each column of switches in turn is read in the same way.

If an operated switch is identified, the microprocessor F preferably checks the identification before it acts to initiate an appropriate predetermined control operation. Checking is achieved by reading the whole array of switches, as described above, a predetermined plurality of times to see that the switch continues to inhibit the output pulse. Operation of each switch produces a unique identifying code which is stored in the microprocessor when it is first produced and is compared with the codes produced during successive checking cycles, the appropriate control operation being initiated only after coincidence is registered in a predetermined plurality of successive comparison operations.

As well as identifying operation of one particular touch switch, the microprocessor can be arranged to identify the simultaneous operation of two or more touch switches and use this to initiate further control operations.

As well as producing 'read' pulses to sense the state of the switches, the microprocessor produces illumination control signals that are applied to the electrodes E of the switches to control illumination of each. This is achieved by applying an illumination control signal to all of the electrodes E of the switches in each row in succession via respective illumination input terminals SL1 to SL4, this being done in timed sequence with the application of pulses to the input terminals SC1 to SC4 so that the illumination of each switch is controlled individually. The illumination control signals are produced by the microprocessor in the required sequence at four outputs of an input/output port I/O2 and pass via an amplifier IC3 to the terminals SL1 to SL4. The electrodes E in each row are connected together via their input connections SL and are connected to the respective terminals SL1 to SL4.

The input pulses applied to terminals SC1 to SC4 in sequence with the illumination control signals to terminals SL1 to SL4, may be the 'read' pulses, mentioned earlier, that are analysed to sense whether or not any of the switches have been operated. Preferably, however, these pulses to terminals SC1 to SC4 are produced independently of the 'read' pulses and the microprocessor controls the sensing of operated switches and the illumination of the switches separately of one another.

The microprocessor F must possess instructions enabling it to perform the requisite con-

secutive output/input operations at a speed necessary for the above-described functions, and an example of a suitable microprocessor is the Fairchild F-8.

5 The array of switches illustrated in Fig. 2 is preferably constructed on a single dielectric panel G to which the individual conductive layers A, B, C of the switches are applied. Also, it is advantageous in such a unitary  
10 construction to provide a common electrode E for each row of switches so that just a single input connection SL is required for each row for connection to a respective terminal SL1 to SL4. This can readily be achieved in Fig. 2 by  
15 arranging the layers B and C one above the other rather than alongside one another, and providing a single strip electrode E that extends along the row across the layers B but not across the layers C.

20 Although a square  $4 \times 4$  array of switches has been illustrated, it will be appreciated that the array may comprise any symmetrical or non-symmetrical array of  $n$  groups of  $m$  switches with  $m$  read inputs, each of which is  
25 connected to a respective set of said switches comprising one from each group,  $n$  read outputs, each of which is connected to all of the switches of a respective group, and  $n$  illumination control inputs, each of which is con-  
30 nected to all of the switches of a respective group.

The illustrated array of touch control switches may be incorporated in an hermetically sealed housing. Also, a printed circuit  
35 board incorporating interfacing circuitry such as the circuits IC1, IC2 and IC3 may be mounted on the rear of the dielectric panel G.

#### CLAIMS

40 1. A matrix array of touch control switches arranged in  $n$  groups of  $m$  switches in each group, with  $m$  'read' inputs, each of which is connected to a respective set of said switches comprising one from each group, and  $n$  'read'  
45 outputs each of which is connected to all the switches of a respective group; and a processor connected to the said 'read' inputs and outputs and acting so as to apply a 'read' signal to each of the inputs in succession and  
50 to analyse the resultant signals appearing at the outputs on each application of the 'read' signal and thereby to determine whether any of the respective set of switches is in an operated state.

55 2. A matrix array according to Claim 1 in which the processor is arranged to apply each 'read' signal a predetermined plurality of times comprising a 'read' cycle so that the processor reads the state of each set of  
60 switches that plurality of times and only responds if the same pattern of signals corresponding to a control function occurs at the 'read' outputs each time.

65 3. A matrix array according to Claim 1 or Claim 2 in which each 'read' signal is a pulse

signal and a corresponding 'read' pulse appears at the output of each switch, but at the output of a switch which is in an operated state the amplitude of the output pulse is  
70 reduced, and each 'read' output is connected to the processor via a circuit that passes the signal to the processor only if it is above a predetermined threshold corresponding to the lower limit of amplitude of 'read' output pulse  
75 signals from a switch that is in a non-operated state.

4. A matrix array according to any one of Claims 1 to 3 in which each switch comprises first and second conductive layers arranged on  
80 opposite sides of a dielectric panel in superimposed relationship to one another, with an electric input connection to the second conductive layer for connection to the respective 'read' input, a phosphor layer in contact with  
85 the second conductive layer, and an electrode superimposed on the phosphor layer, the first and second layers and the dielectric panel being transparent so that when the phosphor layer is excited by the application of a potential between the second layer and the electrode it is visible through the first layer.

5. A matrix array according to Claim 4 including  $n$  illumination control inputs, each connected to the said electrodes of all the  
95 switches of a respective group, and the processor being connected to the 'read' inputs and the illumination control inputs so as to be able to apply signals thereto to illuminate selected switches.

100 6. A matrix array according to Claim 4 or Claim 5 in which the dielectric panel is common to all the switches of the array and the electrodes of the group are formed by a single respective electrode.

105 7. A matrix array of touch control switches with inputs and outputs connected to a microprocessor substantially as herein described with reference to Fig. 2 of the accompanying drawings.